Roll No……..….. **Total No. of Printed Pages: 1**

Total No. of Questions: [11]

MCA (Semester –3rd)

DIGITAL CIRCUITS & LOGIC DESIGN

Subject Code: MECE0F95

Paper ID: [OE1270124]

Time: 03 Hours **Maximum Marks: 60**

Instruction for candidates:

1. Section A is compulsory. It carries 16 marks. It consists of 4 questions of 4 marks each.
2. Section B consist of 4 questions of 8 marks each. The student has to attempt any 3 questions out of it.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

Section – A **(4 marks each)**

Q1. Write De-Morgan's theorem. Minimize using Boolean algebra wxyz + x'yz + yz' + wx

Q2. Differentiate between RTL, ECL and TTL logic families.

Q3. Write truth table of 3-input NOR gate.

Q4. Design circuit diagram for Half Subtractor.

Section – B **(8 marks each)**

Q5. Implement the following function using Decoder

F(A,B,C,D) = ∑m (0,1, 2, 3, 6, 7,8,12,15)

Q6. Design BCD to 7 Segment Display.

Q7. What are Flip-flops. How Master slave flip flop is used to avoid Race Around condition.

Q8. Write short note on PAL, PLA, CPLD & FPGA.

Section – C **(10 marks each)**

Q9. Describe various characteristics of D/A convertor. Also explain the working of R-2R D/A convertor.

Q10. What are counters. Design MOD 7 counter using JK flip flop.

Q11. Minimize using K Map technique F(w,x,y,z) = ∑m (2,3,4,5,7,8,9,11,12, 13)+ d(6,10)