

# Effects of Prefetching with and without Exclusive Ownership - ROUGH DRAFT

John Paul Harriman and Alex Goberna

## Summary

We examined and verified methods of software prefetching with and without exclusive ownership to view the benefits and drawbacks of implementing as opposed to hardware prefetching.

## Background

Key data structures -

Operations on these structures -

Algorithms inputs and outputs -

Computations expensive and benefit from parallelization

Workload breakdown, dependencies, parallelism, data-parallel, locality, amenable to SIMD

Prefetching - what it is

Architecture of x86

With ownership cache coherency for multicore

Pitfalls of prefetching

# Approach

Technologies - gem5, ramulator

Mapped problem to target parallel machines

Change original serial algorithm to enable better mapping to a parallel machine?

Describe process of iterations

Existing code -

# Results

# Future Work

ML approach

# References

[http://www.cs.cmu.edu/afs/cs.cmu.edu/user/tcm/www/thesis/subsection2\\_9\\_1\\_3.html](http://www.cs.cmu.edu/afs/cs.cmu.edu/user/tcm/www/thesis/subsection2_9_1_3.html)

<http://learning.gem5.org/book/>

[http://users.ece.cmu.edu/~omutlu/pub/ramulator\\_dram\\_simulator-ieee-cal15.pdf](http://users.ece.cmu.edu/~omutlu/pub/ramulator_dram_simulator-ieee-cal15.pdf)

[http://users.ece.cmu.edu/~omutlu/pub/eaf-cache\\_pact12.pdf](http://users.ece.cmu.edu/~omutlu/pub/eaf-cache_pact12.pdf) - read

# Work and Credit

Journal:

11/22:

Gem5 update

- Gem5 installation and onboarding was more complicated than initially expected, especially after having to use a VirtualMachine just to get started.
- Preferred Gem5 over ZSim because we are able to maintain a full system integration while still keeping track of core metrics, as opposed to ZSim which doesn't maintain a full system.
- Using X86 Processor instead of ARM because we are able to use the prefetching Intel commands already built without having to craft our own
- Completely missed the point of what prefetching with ownership meant, realized that it means the protocol doesn't change, the request the prefetcher makes changes

Prefetching Notes ref [here](#)

- Prefetching follows a similar protocol to that of cache coherence, which initially sparked our mistake. Memory can have shared access, or exclusive access. Prefetching is the same, except that it will either fetch a shared copy of a line, or an exclusive copy.
- Benefits of the exclusive mode prefetching can be
  - Reducing latency of the subsequent write, depends on write buffers of system
  - Read-Modify-Write cases where processor asks for shareable copy then an exclusive copy. This reduces requests to 1 which potentially has the effect of cutting down half of all memory traffic. Which reduces contention.