Board Design Notes

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Here are some general rules to follow for PCB design. This document started when I was an undergrad and has expanded over the years. It assumes Eagle CAD but most of the ideas are generalizable.

Table of Contents:

Schematic Rules

BOM rules

Layout Rules

Libraries

Links and Resources

Schematic Rules

Here I use the term "nets" to mean wires or busses

Absolutely Required

- Name important and externally accessible nets
- Put notes in for confusing parts of the design
- Proper use of junctions (brown or green circles for joining of 3 or more segments)
- Parts must have names and values, if appropriate.
- Decoupling .1uF caps near power of every IC

If at ALL possible

- Only vertical and horizontal lines should be used for nets
- Separate sheets to group parts of the design, with connections made by common net names that are clearly labeled
- Use power port symbols for power rails
- No two pins directly connected or parts overlapping (connect with longer nets), or text overlapping
- Pass all important ERC errors (look in messages panel or tools menu)
- Pay attention to all ERC warnings (especially make sure that all of your junction dots are actually connected. They can look connected visually but may not be electrically connected)

Very Good Ideas

- Name and label every single net
- "Left to right" layout (i.e. input on left, output on right)
- Name components something better than U$1 (good names are like D1 for diodes, while U$1 could be anything)
- Put notes in about layout restriction (like "These two parts must be close together!", etc)
- Avoid crossing nets if possible
- Do not use nanofarads (nF), instead use pF for 9,999 pF (9.9nF) and below, and uF for .01uF (10nF) and above .

BOM rules

- For each non-generic part (a standard resistor or capacitor, for which there are multiple reasonable options, counts as generic), add the following Eagle attributes (right click the part in the schematic -> Attributes):
    - MPN (manufacturer part number, complete with any qualifiers till there is no ambiguity about the package/temperature spec etc.--look in the datasheet for this)
    - (Optionally, if there are various manufacturers for the part) MF (manufacturer),
    - At least one of: DIGIKEY (Digikey part number), MOUSER (Mouser part number), ARROW (Arrow part number) in that order of preference
    - Eg: for the AS5040 encoder chip, set MPN = AS5040, and DIGIKEY = AS5040-ASSTCT-ND; for the ATmega32u4 MCU on XBM 3.1, set MPN = ATmega32U4-AU (note that the -AU at the end is required to disambiguate the package), and DIGIKEY = ATMEGA32U4-AURCT-ND
- For capacitors, add attribute VOLTAGELEVEL (the nominal operating voltage of the capacitor), with ONLY the following options for the value: 5V, 40V. These will be doubled when speccing the part on Digikey.

Layout Rules

Absolutely Required

- 6 mil line width/spacing, more for high current traces (check with specific board manufacturer)
- High current path must be completely connected with wider traces and kept as short as possible
- Make sure the board fits in the space needed, including connectors in accessible places, etc
- For decoupling caps and other components in parallel, place them near the other features they are near in the schematic. (i.e. if you have a cap C1 near IC1 and C2 near IC2 in the schematic, they should not be switched in the layout).
- Make sure decoupling capacitors are physically near the net that they are filtering
- Pass all important DRC errors (Tools, Design Rule Check)
- Check to make sure there are no parts under other parts, especially connectors.

If at ALL possible

- 10 mil line widths
- Ground planes everywhere, with the possible exception of near switching nodes (add vias to extend the ground plane)
- No right angle turns especially for <= 12mil widths
- No random angle traces (i.e. only at angles at a multiple of 45 degrees), and especially no acute angles (even going into a pad).
- Keep noise sensitive traces short and avoid running them over/under high current traces, including any analog inputs, high-z nets, gate lines on fets, etc.
- Use a "Kelvin Connection" for current sense resistors. Basically both sides should come together and run parallel to each other. They should also come out of the opposite side of the pad as the high current trace.
- Run a dedicated VCC and GND connection between decoupling caps and ICs.
- Give a short but meaningful name to the board and write it in silk screen along with revision number. If you are ordering a board without silk screen, write it in copper.
- Set isolate to at least 10mils for all polygons unless smaller is necessary to connect two polygons
- Silk screen designation for polarity of diodes, etc
- Silk Screen box for serial number
- Pin 1 indicators even for headers need to be correct, including square pads.
- Signal pairs (like 485 A/B, camera/GND, etc) should be routed along parallel traces as close to each other as possible, and roughly the same length. Don't put anything between them. Also don't run any other traces parallel to the pair (including other pairs) (put gnd plane between if needed).

Very Good Ideas

- Traces should exit pads in the center and go straight out for at least 10 mils before hitting a via or making a turn
- Avoid all Y and T junctions, especially in smaller traces. Instead route to a 2nd side of a nearby pad on that net.
- Put a silk screen label on everything, and use larger fonts for connections that a user will have to deal with.
- Components should have a silk screen outline of the case body, with pin 1 designation, with nothing over the actual pads (mask and silk layers should be mutually exclusive).
- Have test points available on any net you might ever want to look at while debugging the board. Vias make great test points, as do through hole or larger smt pads. (Space permitting)

Libraries

Absolutely Required

- Meaningful and understandable device/package/variant names
- Any new libraries must be committed to the repository when any board that uses them is

- Stop and cream layers must be correct. (soldermask and solderpaste layers)
- Pin 1 indicator as needed (square hole, silk screen dot, mitered corner, etc)
- Packages must be able to pass DRC when used on a board (i.e. no 1mil trace widths, etc)
- Double check dimensions and units!!

If at ALL possible

- >NAME and >VALUE tags on Symbol, Package
- Set direction on all pins in symbol (I/O, PWR, etc)
- Descriptions set for package and devices
- Origin is in predictable location (i.e. in the center) for all parts of library
- Parts broken into small library files by manufacturer or device type--not name of creator, etc
- No silk screen (place, name, value layers) should overlap pads (or stop layer)--that is what the docu layer is for (among other things). Some bad board houses will print it over the copper...
- Use pads and not just rectangles. If you do use rectangles, double check stop and cream layers

Very Good Ideas

- Set swaplevels
- Symbol should imply functionality graphically, i.e. make it look like a transistor if it is a transistor
- Symbol should be as compact as is reasonable, but should be on roughly the same scale as other parts we use (i.e. not greatly larger or smaller than other similar parts)
- Attributes set as appropriate

Links and Resources

- NASA Soldering Standard - https://workmanship.nasa.gov/lib/insp/2%20books/links/sections/701%20General%20Requirements.html
- Kelvin Conection - https://en.wikipedia.org/wiki/Four-terminal_sensing