Ashan Shanaka Liyanage

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Languages : Sinhala (Native), English (Fluent), German (A2)

Education

- Technische Universität Darmstadt, Germany

  The International Master Program – Information and Communication Engineering (2016 Oct. - present)

- University of Moratuwa, Sri Lanka

  B.Sc. Electronic and Telecommunication Engineering (2009-2014)

Publications

- S. Mallawaarachchi, K. Wimalana, A. Liyanage, G. Premalal, S. Samarasinghe, and N. D. Nanayakkara, "Automating whole slide imaging using an arduino platform," in 8th international conference on Biomedical Engineering (BMEiCON), (Pattaya, Thailand), IEEE, Nov. 2015.

- S. Mallawaarachchi, G. Premalal, K. Wimalana, A. Liyanage, S. Samarasinghe, and N. D. Nanayakkara, "Detection of microfilariae in peripheral blood smears using image analysis," in Industrial and Information Systems (ICIIS), 2013 8th IEEE International Conference on, (Peradeniya, Sri Lanka), pp. 300–303, IEEE, Dec. 2013.

Working Experience

- Synopsys, Sri Lanka : Corporate Application Engineer
  (Mar. 2014 – Sep. 2016)

  Validated static low power (LP) tools 'VCLP' and 'Spyglass' - System on Chip design verification tools.
  Worked on LP projects and features related to LP Strategies, command and options. Analysing and validating customer designs.
  Design development at RTL,Netlist and PG Netlist stages. Automated Benchmark processes and report generating.

- CRISP (Center for Research in Security and Privacy) Lab, Darmstadt : Student Employee (June 2017 – Sep. 2017)

  Design and integration of a BLAKE 2b Hash Controller interface and a hash simulator using Verilog for control flow attestation on the PULPino processor.
  (Verilog, SystemVerilog, PULPino, toolchain)

Mini Projects (recent)

- List scheduler for pipelined FUs (Jan. 2018)

  Implementation of a List scheduling algorithm which supports different priority criteria. (High Level Synthesis, Scheduling Algorithms, Java)

- Processor with Multiple pipeline stages (Aug. 2017)

  Implementation, Verification, Gate-Level sythesize and Simulation of a Pipelined Processor of ARM THUMB instruction set architecture which execute given binary instructions. (Verilog, Modelsim, Design Compiler)

Achievements

- 2013: Dean's list for semester 7 and 8 at University of Moratuwa.
- 2012: Runner-up All Island IESL robot competition - the annual island wide robotic competition.
- Ranked 61 in Sri Lanka (out of 50,000+ candidates) in GCE A-Level (university entrance) exam in 2008.
- Full merit scholarship from Sri Lankan government for undergraduate studies.

Competencies

- Verilog, SystemVerilog
- Digital circuits design, simulation (behavioural and Gate-level), Verification
- Microprocessor Architectures (ARM, LEON3, UTLEON3)
- Low power design Methodologies, UPF
- TCL, Shell, Perl, Python
- Assembly, C/C++, OpenCL, Scala, Java
- Matlab and Simulink
- Modelsim, Design Compiler, VCLP, SpyGlass, Virtuoso, Liberate
- Git, Perforce
- vim/gvim
- Red Hat Enterprise Linux, Ubuntu, Windows
- Arduino, FPGA (virtex-5, Cyclone-III)
- HTML, CSS, JavaScript, php
- LaTeX
- Adobe PhotoShop, Illustrator, InDesign, Video Production