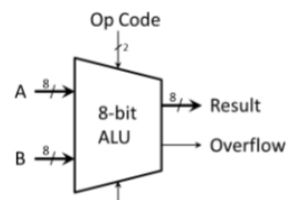
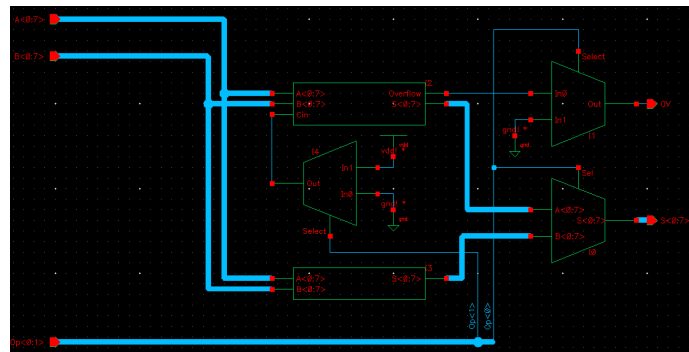


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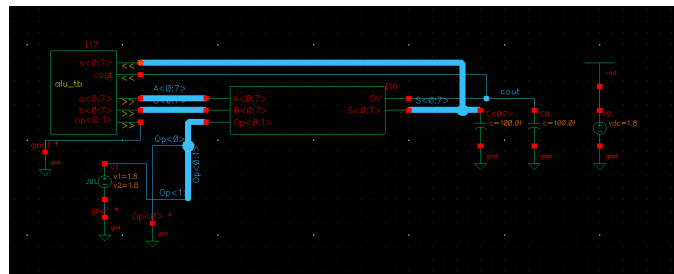
8-Bit ALU

Schematic

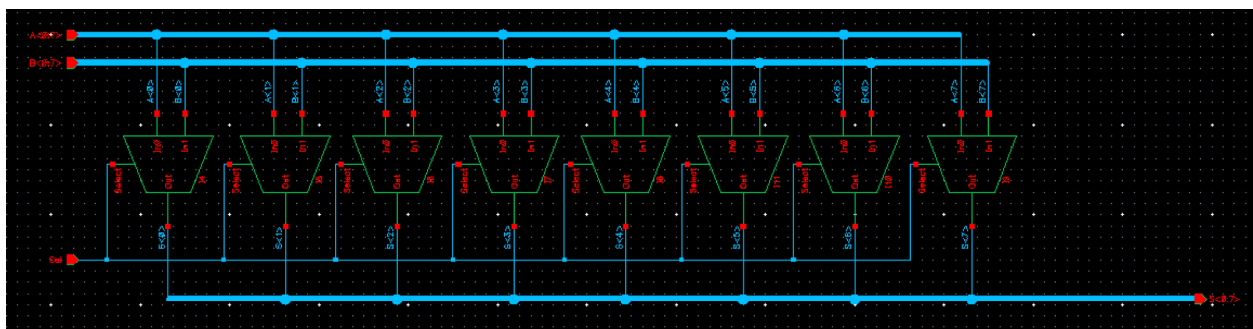


Op Code Functions
00 Addition (A+B)
01 Subtraction (A-B)
10 <Your Choice>

Testing Framework

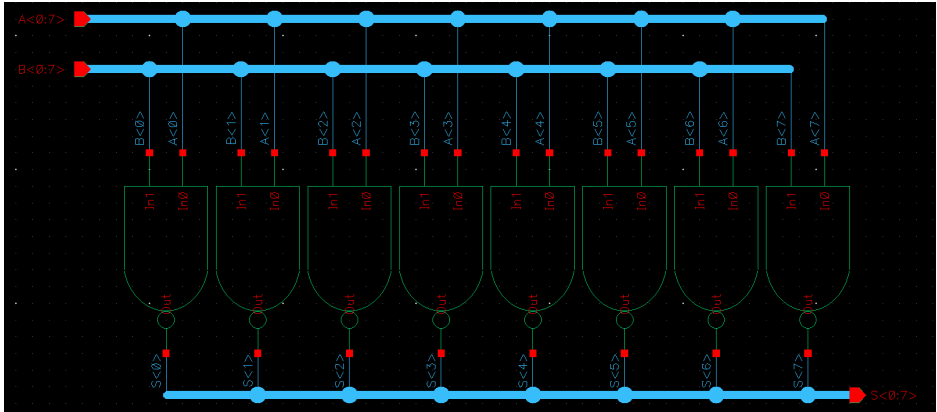


8-Bit MUX module

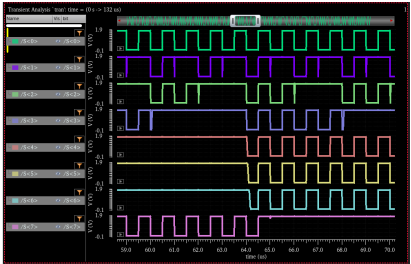
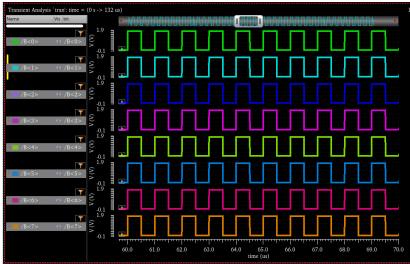
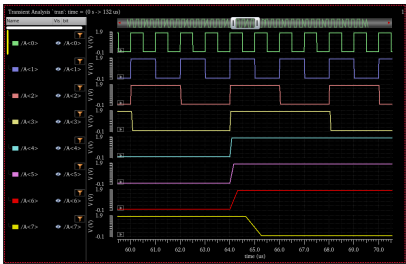


10 Operation: NAND

8-Bit bitwise NAND module

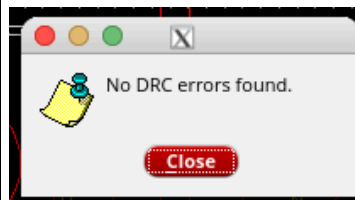
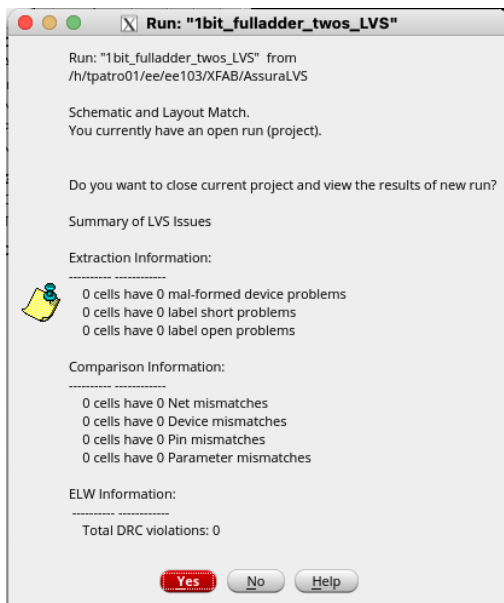
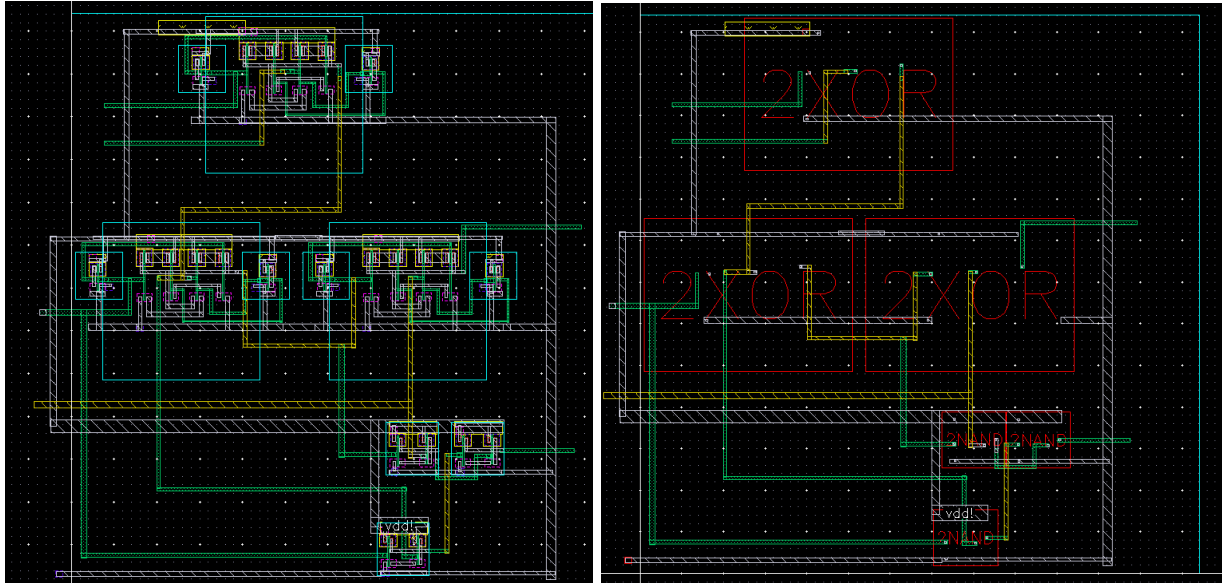


Testing op code: 10 component



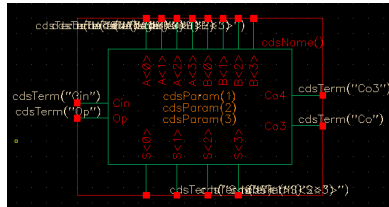
time	60.0	61.0	62.0	63.0	64.0	65.0	66.0	67.0	68.0
A	11100001	10100001	11000001	10000001	11111111	10111110	11011110	10011110	11101110
B	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
S	00011110	01011110	00111110	01111110	00000000	01000001	00100001	01100001	00010001

1-Bit Full Adder with Two's Complement

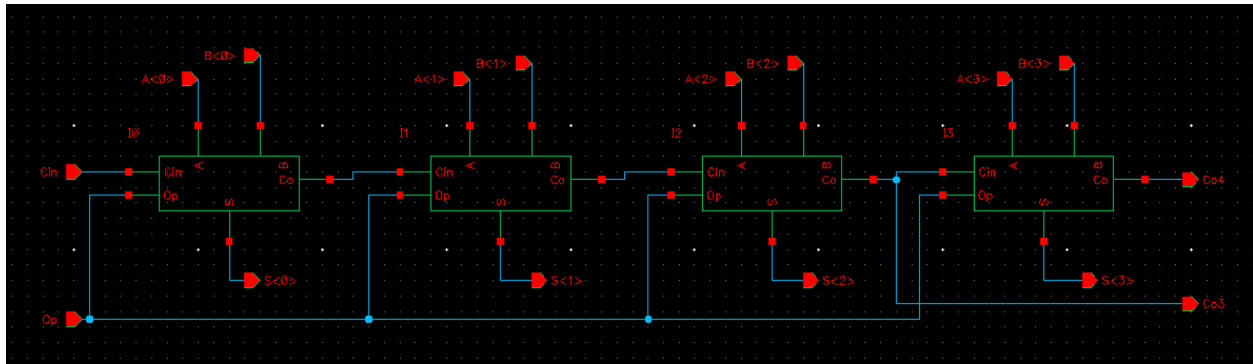


4-Bit Full Adder Module

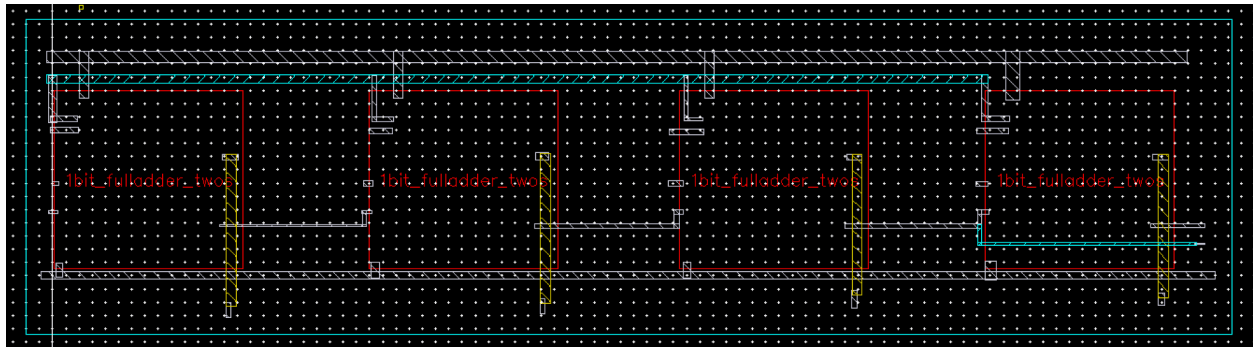
Symbol



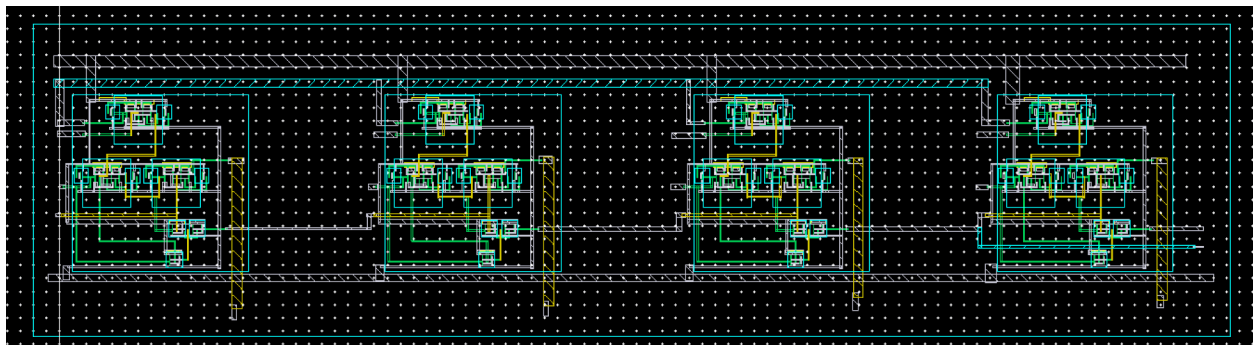
Schematic



Overall Layout

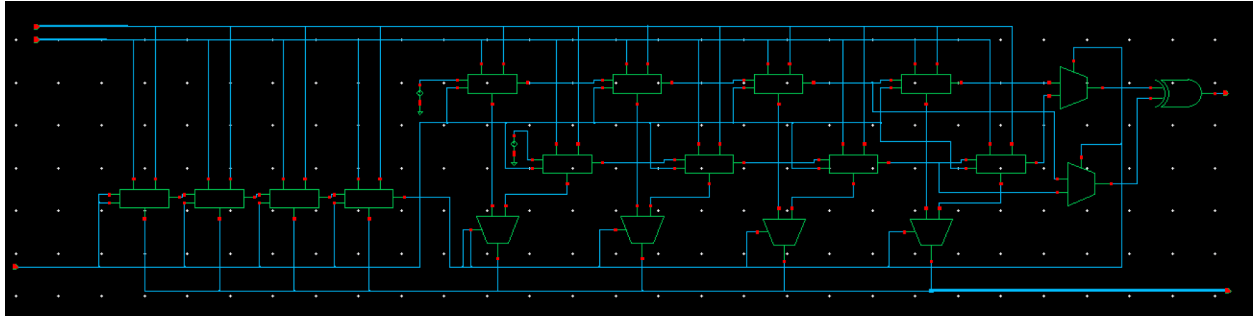


Layout with transistors visible

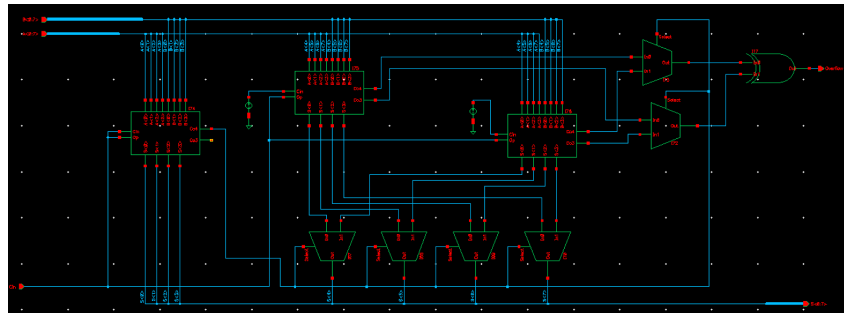


8-Bit Full Adder with 4-Bit Carry Select

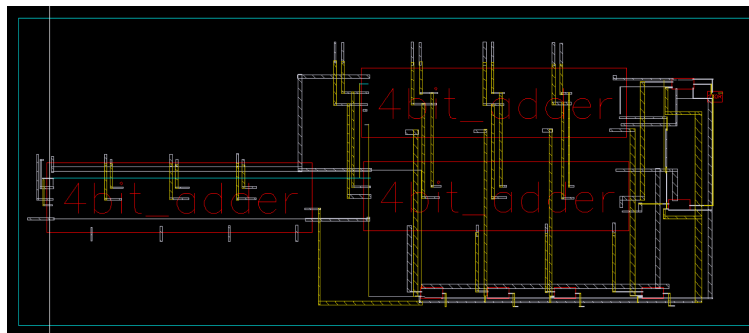
Original Schematic without 4-Bit Adder Modules



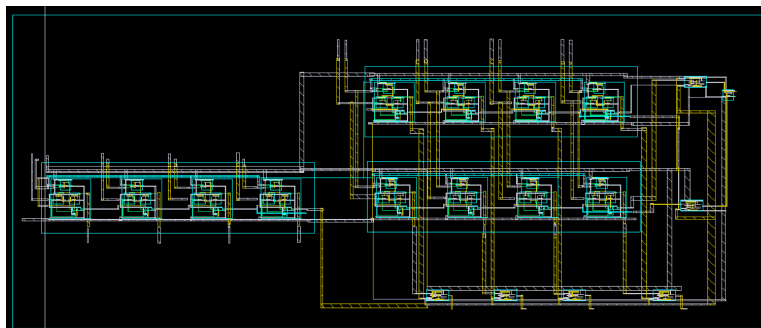
Schematic Implemented for Layout



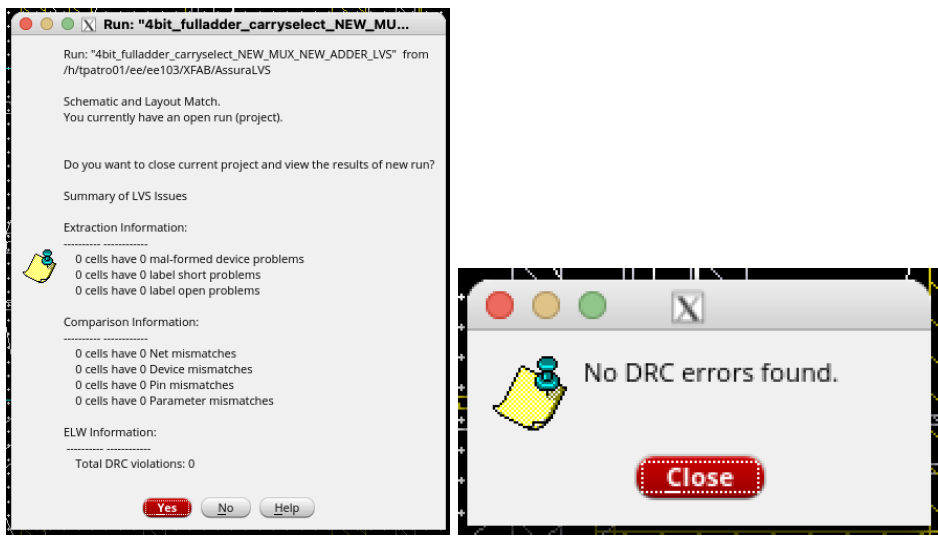
Top Level of Layout



Overall Layout



Results

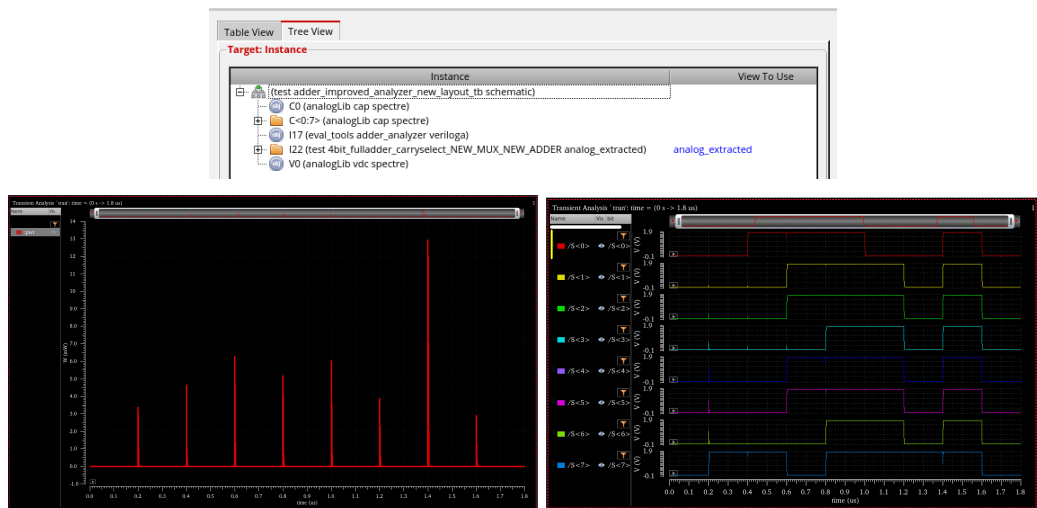


Test Results (100 fF)

Generated by Spectre from `I17'

127	+	1	=	-128 (OF=1)	PASS	delay: 2.77 ns
-128	+	1	=	-127 (OF=0)	PASS	delay: 2.22 ns
56	-	1	=	55 (OF=0)	PASS	delay: 2.03 ns
55	-	56	=	-1 (OF=0)	PASS	delay: 2.17 ns
-1	-	1	=	-2 (OF=0)	PASS	delay: 1.81 ns
-1	-	127	=	-128 (OF=0)	PASS	delay: 2.18 ns
127	+	-128	=	-1 (OF=0)	PASS	delay: 2.27 ns
0	+	0	=	0 (OF=0)	PASS	delay: 1.88 ns

Test Results (10 fF)



Overall the layout does match the schematic so functionally they are the same. As expected however, the layout uses more power due to the calculable losses from having measurable areas. The overall differences with power and delays definitely make sense. I think the layout could have been improved by using less area and better optimizing for area. This would have lowered resistance and then use less power overall.

	Worst case input conditions	Worst case delay (ns)	Maximum Operating Frequency (MHz)	Static Power (pW)	Avg. Dynamic Power @ 5MHz (uW)	Number of Transistors	Area (sq. um)
Carry Ripple	127 + 1	3.07	325	6.79	3.88	100	
4-bit Carry Select	127 + 1	2.77	361	9.43	5.64	490	
4-bit Carry Select Post Layout	127 + 1	4.23	236	624	9.67	490	25600

Throughout the design process, I learned so much. I thought it was really cool to start off at the schematic transistor gate level and then build up to an “accelerated” adder. I think it was a fairly intuitive design process (even if the tools had a bit of a learning curve). I thought that the tutorial website was incredibly helpful and very clear. Having access to a knowledgeable TA also made the entire process slightly more frictionless.