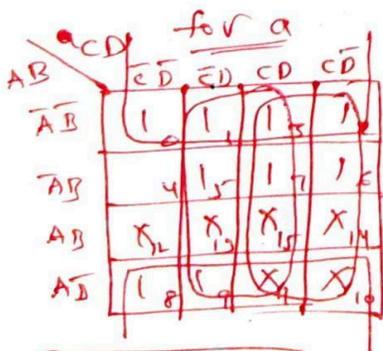


**Q1.**

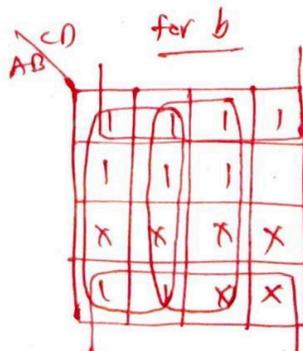
The Last 2 - digits are 46

Truth Table :-

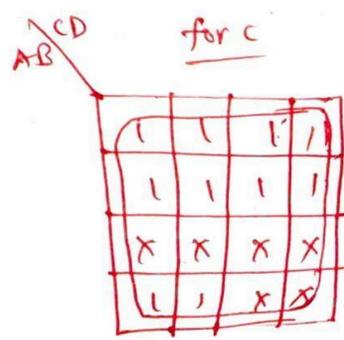
BCD inputs				7 - Segment Display							Symbol
A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	00000000
0	0	0	1	1	1	1	1	1	1	0	
0	0	1	0	1	1	1	1	1	1	0	
0	0	1	1	1	1	1	1	1	1	0	
0	1	0	0	0	1	1	0	0	0	1	
0	1	0	1	1	1	1	1	1	1	0	
0	1	1	0	1	0	1	1	1	1	1	
0	1	1	1	1	1	1	1	1	1	0	
1	0	0	0	1	1	1	1	1	1	0	
1	0	0	1	1	1	1	1	1	1	0	
1	0	1	0	x	x	x	x	x	x	x	
1	0	1	1	x	x	x	x	x	x	x	
1	1	0	0	x	x	x	x	x	x	x	
1	1	0	1	x	x	x	x	x	x	x	
1	1	1	0	x	x	x	x	x	x	x	
1	1	1	1	x	x	x	x	x	x	x	



$$a = \bar{B} + C + D$$



$$b = \bar{B} + \bar{C} + D$$



$$c = 1$$

Similarly

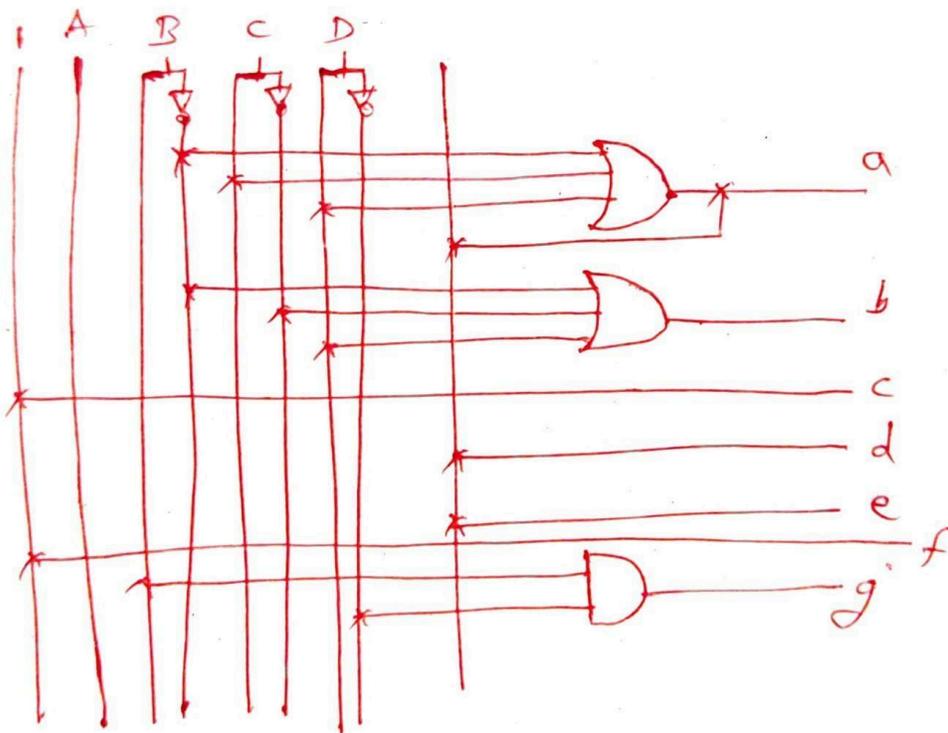
$$d = \bar{B} + c + D$$

$$e = \bar{B} + c + D$$

$$f = 1$$

$$g = B\bar{D}$$

Logic Circuit :-



## **Q2.**

All the D-flip-flop and gates used in the circuit have non-zero propagation delay resulting in spurious transitions or glitches.

These are several ways to eliminate them and they are as follows:

1. Reducing switching activity
2. Gate sizing
3. Gate freezing
4. Gate triggering
5. Multiple threshold transistors