Artaz FLAFRBE Processor All-in One Document
(FLAFRBE = Fast Logic Architecture for Running BF Efficiently)

This document contains information about the Artaz FLARE processor, including its ISA (Instruction Set Architecture), and compiler.

Document begins below.

Artaz FLAFRBE ISA (Instruction Set Architecture)

Definitions

cp **cell pointer**
imm **immediate**
tlp **text location pointer**
tty **tty console**

Opcode	Mnemonic	Operands	Description
1	**CP.INC**		**cp++**
2	**CP.DEC**		**cp—**
3	**ADD**	**imm[0-2[0-15]]**	***cp += imm**
4	**SUB**	**imm[0-2[0-15]]**	***cp -= imm**
5	**LOOP.EN**		**while(*cp != 0){ }**
6	**LOOP.EX**		**End [Loop**
7	**INPUT**		***cp = user input**
8	**OUTPUT**		**tlp++, tty[tlp] = *cp**

Machine Settings Opcodes

9	**OVERFLOW.255**	**Whether to overflow at 255 Using Add/Sub**

Registers

Addressing	Name	Description
1	**CPR**	**Cell Pointer Register**
2	**COR**	**Cell Operation Register**
2	**TLP**	**Text Location Pointer**