UART Design and Verification

PROJECT PHASE 2

Subject code: EC124

Submitted by

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in partial fulfillment of the requirement for the award of degree of

BACHELOR OF TECHNOLOGY



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
PONDICHERRY ENGINEERING COLLEGE
PUDUCHERRY – 605 014

MAY - 2021

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
PONDICHERRY ENGINEERING COLLEGE
PUDUCHERRY – 605 014

BONAFIDE CERTIFICATE

This is to certify that this project report titled **"UART design and verification"** is the bonafide work done by **S.ASHWIN KUMAR(17EC107)**, in partial fulfilment of the requirements for the award of the degree **BACHELOR OF TECHNOLOGY** in **ELECTRONICS AND COMMUNICATION ENGINEERING** during the year 2020-2021.

A.V. Ananthalakshmi 15/05/2021

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Submitted for the university examination held on_____.

INTERNAL EXAMINER **EXTERNAL EXAMINER**

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CERTIFICATE

This is to certify that the project entitled **Design and Verification of UART protocol Using Verilog** was carried out by **Ashwin Kumar S** at **SION SEMICONDUCTORS PVT LTD, BANGALORE** under guidance of **Shaik Chand Basha** during **Feb 2021** to **May 2021**.

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Sr. Technical Manager,
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S. ASHWIN KUMAR(17EC107)

ABSTRACT

A UART (Universal Asynchronous Receiver Transmitter) is typically a piece of hardware on microcontrollers or computers that changes data between serial and parallel forms. It is used for serial communication of data and encompasses a transmitter (which is essentially a parallel to serial converter), a receiver (which is essentially a serial to parallel converter) and both are clocked separately. UART is often connected to the bus of the device that carries parallel data. When a data byte is written to the transmitting data register of a UART by the data-bus, the UART will convert it to serial form and start to transmit the data on the serial line. UARTs are frequently utilized with communication standards like RS-485 or RS-232. Data format and transmission speeds (known as baud rate) are configurable in the UARTs and the electric signaling levels and techniques are commonly taken care of by the driver circuits that are external to the UART.

In this project, design layout is performed for the UART. The UART controller RTL has been developed using Verilog and the test environment was developed using System Verilog. Simulations were carried out using Questasim . QuestaSim is part of the Questa Advanced Functional Verification Platform and is the latest tool in the Mentor Graphics tool suite for Functional Verification. This tool supports advanced Verification features like coverage databases, coverage driven verification, working with assertions, SystemVerilog constrained-random functionality.

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LIST OF ABBREVIATIONS

UART	Universal asynchronous receiver-transmitter
RTL	Register _transfer level
FPGA	Field programmable Gate arrays
SOC	System on chip
IOS	iPhone operating System
AWS	Amazon web service
BIST	Built in self test
VHSIC	Very High-Speed Integrated Circuit.
VHDL	Very high speed integrated circuit hardware description language
PSL	Property Specification Language
UPF	Unified Power Format
IP	Internet Protocol

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

The aim of this chapter is to give a brief description of company profile , overview and the idea of UART Design and verification .

1.2 COMPANY PROFILE

Having its HQs in Bangalore and branch offices in Singapore, Hyderabad and Kochi, SION Semiconductors is a World class company offering complete end-to-end product engineering services such as Chip Design, Embedded Hardware Design, Software & Application development and Product testing & automation.

1.2.1 Product Development Services

Our passionate and diligent team have a wide range of skills across electronic product development and can provide a complete end-to-end services from concept definition till production, for numerous application areas such as Artificial Intelligence, IOT, Autonomous Driving and Data analytics

1.2.2 VLSI Design Services

Our VLSI design team is having immense experience in complete chip design flow from specification to GDSII on latest node technologies such as 7nm, with special focus on RTL/FPGA Design, SoC Verification, Physical Design and FPGA Emulation.

1.2.3 Embedded Design Services

Our Embedded design team has deep expertise in realizing product development from concepts for a wide range of application areas on cutting-edge technologies.

1.2.4 Cloud, IoT and Application Development Services

Our application development team has immense experience in a wide range of application development on Android/iOS platforms and also on developing backend server development including advanced geofencing and low-latency data buffering implementations on Google IoT cloud and Amazon AWS platforms.

1.3 OVERVIEW

A UART (Universal Asynchronous Receiver Transmitter) is typically a piece of hardware on microcontrollers or computers that changes data between serial and parallel forms. It is used for serial communication of data and encompasses a transmitter (which is essentially a parallel to serial converter), a receiver (which is essentially a serial to parallel converter) and both are clocked separately. UART is often connected to the bus of the device that carries parallel data. When a data byte is written to the transmitting data register of a UART by the data-bus, the UART will convert it to serial form starts to transmit the data on the serial line. UARTs are frequently utilized with communication standards like RS-485 or RS-232. Data format and transmission speeds (known as baud rate) are configurable in the UARTs and the electric signaling levels and techniques are commonly taken care of by the driver circuits that is external to the UART

1.4 OBJECTIVE

The objectives are:

- The main objective of this project is to develop a UART design .
- The UART controller RTL(will be developed using Verilog and the test environment will be developed using System Verilog)
- Verification of Integrated Circuits using Verilog lacks the flexibility and reusability of the environment.
- System Verilog provides building blocks and OOP concepts to work with. That allows to create much more flexible test environment with reusable components
- This project presents a verification architecture of configurable Verification IP for UART interface

1.5 ORGANISATION OF THE DISSERTATION

The report has been organized in such a way that each chapter deals with the major perceptions involved in this project.

CHAPTER 1 : This chapter deals with background, motivation and objective of the project.

CHAPTER 2: This chapter reviews the literature of the existing system methodology for the development of UART.

CHAPTER 3: This chapter deals with the detailed explanation of the proposed system

CHAPTER 4: This chapter depicts the results of the simulation and synthesis.

CHAPTER 5: Chapter 5 concludes the proposed work and also presents the recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

The literature review elaborates the work that has been done in this field previously and compares them.

2.2 EXISTING FEATURES AND METHODOLOGY STUDY

1. Further, design systems without full testability are open to the increased possibility of product failures and missed market opportunities. Also, there is a need to ensure the data transfer is error proof. In this work, introduction of Built-in self-test (BIST) and status register for UART to overcome the above two constraints of testability and data integrity has been proposed.

2. This work presents the basic implementation of the UART module using FPGA and its implementation on Spartan 6. This work aims at designing of various modules in an efficient manner that needs to be embedded in a smaller area, with less consumption of power and improvement in overall integration.

3. UART can be implemented in several ways according to the application required by the designer. This work presents the review on such different techniques which were used with UART for reliable data transmission.

4. This work presents the design and implementation method of a Universal Asynchronous Receiver Transmitter (UART) using VHSIC Hardware Description Language (VHDL). UART has been implemented as a picoblaze processor which can be implemented in large systems and thus has high flexibility in FPGA based design.

5. This work presents implementation of UART with single error correction using Systemverilog. The design was implemented in spartan 6 FPGA.

6. The proposed work presents the design of 9-bit UART modules based on Verilog HDL. This design features automatic address identification in the character itself. The VLSI design of the module has been implemented and passed the data between the proposed 9-bit UART module with a host CPU.

2.3 LITERARY - CONCLUSION

In conclusion, the design and features required for the UART is derived from the literature study.

CHAPTER 3
PROPOSED SYSTEM

3.1 INTRODUCTION

This chapter describes the functioning of UART. UART Stands for Universal Asynchronous Transmitter Receiver. The function of UART is conversion of parallel data (8 bit) to serial data. UART transmit bytes of data sequentially one bit at a time from source and receive the byte of data at the destination by decoding sequential data with control bits. As the entire processes require no clock input from source hence it is termed as asynchronous communication. In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controlling device like a CPU into serial form, transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving device. Only two wires are needed to transmit data between two UARTs. Data flows from the Tx pin of the transmitting UART to the Rx pin of the receiving UART.

3.2 WORKING OF UART

The UART that is going to transmit data receives the data from a data bus. The data bus is used to send data to the UART by another device like a CPU, memory, or microcontroller. Data is transferred from the data bus to the transmitting UART in parallel form. After the transmitting UART gets the parallel data from the data bus, it adds a start bit, a parity bit, and a stop bit, creating the data packet. Next, the data packet is output serially, bit by bit at the Tx pin. The receiving UART reads the data packet bit by bit at its Rx pin. The receiving UART then converts the data back into parallel form and removes the start bit, parity bit, and stop bits. Finally, the receiving UART transfers the data packet in parallel to the data bus on the receiving end. UART transmitted data is organized into *packets*. Each packet contains 1 start bit, 5 to 9 data bits (depending on the UART), an optional *parity* bit, and 1 or 2 stop bits.

UARTs transmit data *asynchronously*, which means there is no clock signal to synchronize the output of bits from the transmitting UART to the sampling of bits by the receiving UART. Instead of a clock signal, the transmitting UART adds start and stop bits to the data packet being transferred. These bits define the beginning and end of the data packet so the receiving UART knows when to start reading the bits. When the receiving UART detects a start bit, it starts to read the incoming bits at a specific frequency known as the *baud rate.* Baud rate is a measure of the speed of data transfer, expressed in bits per second (bps). Both UARTs must operate at about the same baud rate. The baud rate between the transmitting and receiving UARTs can only differ by about 10% before the timing of bits gets too far off. Both UARTs must also be configured to transmit and receive the same data packet structure.

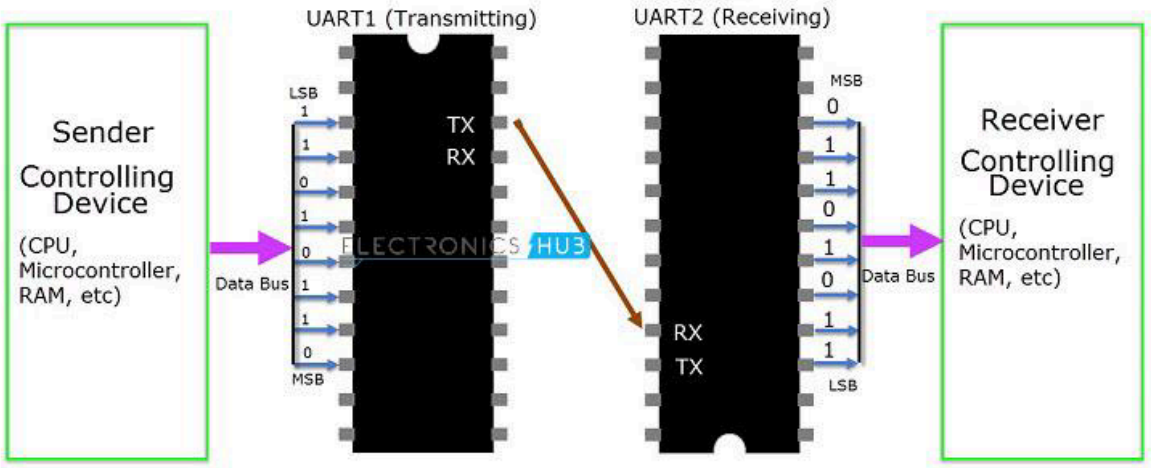


Fig. 3.1 Working of UART

3.3 STEPS INVOLVED IN UART TRANSMISSION

- The transmitting UART receives data in parallel from the data bus.
- The transmitting UART adds the start bit, parity bit, and the stop bit(s) to the data frame.
- The entire packet is sent serially from the transmitting UART to the receiving UART. The receiving UART samples the data line at the pre-configured baud rate.
- The receiving UART discards the start bit and stop bit from the data frame.
- The receiving UART converts the serial data back into parallel and transfers it to the data bus on the receiving end.

3.4 ADVANTAGES OF UART

- Only uses two wires
- No clock signal is necessary
- Has a parity bit to allow for error checking
- The structure of the data packet can be changed as long as both sides are set up for it
- Well documented and widely used method.

3.5 APPLICATIONS OF UART

You can use UART for many applications, such as:

Debugging: Early detection of system bugs is important during development. Adding UART can help in this scenario by capturing messages from the system.

Manufacturing function-level tracing: Logs are very important in manufacturing. They determine functionalities by alerting operators to what is happening on the manufacturing line.

Customer or client updates: Software updates are highly important. Having complete, dynamic hardware with update-capable software is important to having a complete system.

Testing/verification: Verifying products before they leave the manufacturing process helps deliver the best quality products possible to customers.

3.6 SUMMARY

UART or Universal Asynchronous Receiver Transmitter is a serial communication device that performs parallel – to – serial data conversion at the transmitter side and serial – to – parallel data conversion at the receiver side. It is universal because the parameters like transfer speed, data speed, etc. are configurable. UART is a piece of hardware that acts as a bridge between the processor and the serial communication protocol or port. In Asynchronous mode, there is no clock signal to synchronize or validate the data transmitted from the transmitter and received by the receiver (Asynchronous Serial Communication). In UART, the transmitter and receiver must agree on timing parameters beforehand. Also, UART uses special bits at the beginning and ending of each data word to synchronize the transmitter and receiver. More about these special bits in the later sections. The transmitting UART receives parallel data from the CPU (microprocessor or microcontroller) and converts it into serial data. This serial data is transmitted to the receiving UART. The receiving UART, upon receiving the serial data, converts it back to parallel data and gives it to the CPU.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 INTRODUCTION

This chapter deals with software description and the results obtained. The analysis is being done to show that the proposed system is better and more accurate compared to the existing system.

4.2 QuestaSim

QuestaSim or Questa Advanced Simulator is software from Mentor Graphic company that is provided for simulation, programming testing and debugging of FPGA and SoC chips. The program supports many hardware description languages such as Verilog, SystemVerilog, VHDL, SystemC, PSL and UPF, and with various tools that provide you with the ability to test the programming of the above chips before the actual design and implementation Gives. Questa Simulator is the core of Questa's comprehensive simulation and debugging platform, which reduces the risk of evaluating these chips.

4.2.1 QuestaSim FEATURES

- High efficiency and support for several hardware description languages
- Efficient and advanced evaluations
- Easy to use and fast debugging
- Automatic production of tests
- Multi-core simulation and parallel testing

4.4 MODULES DESCRIPTION

4.4.1 BAUD RATE GENERATOR

The baud rate generator consists of clk_ash as input and rxclk_en and txclk-en as output where rxclk_en oversamples by 16x.

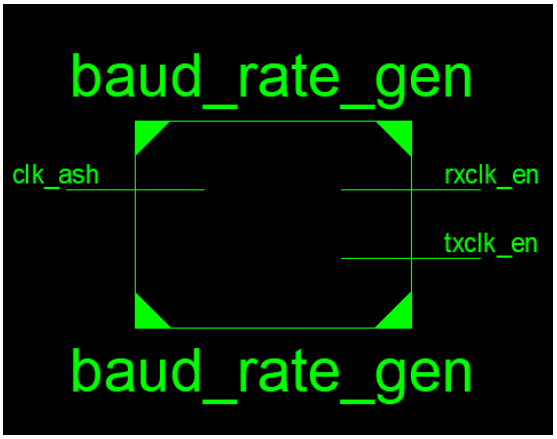


Fig.4.1 RTL Schematic

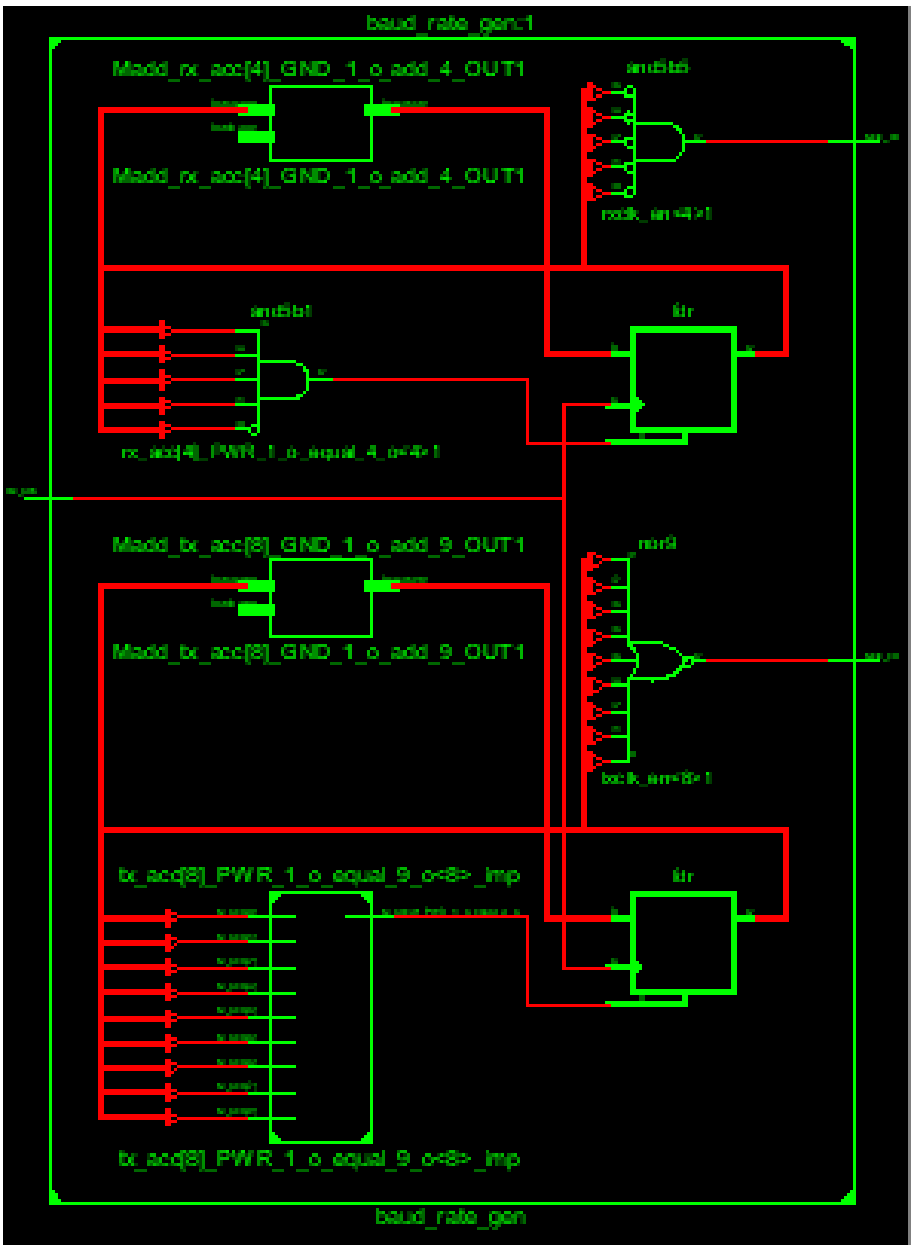


Fig.4.2 Expanded RTL Schematic

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
IOs									
txclk_en	0.00000	LVCMOS25_12_SLOW	0.0	0.3	Async	Async	0	1	0
rxclk_en	0.00000	LVCMOS25_12_SLOW	0.0	3.1	Async	Async	0	1	0
clk_50m	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
Total	0.00000					Count	1	2	0

Fig.4.3 I/O Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx9csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              14  out of  11440     0%
 Number of Slice LUTs:                   28  out of   5720     0%
    Number used as Logic:                28  out of   5720     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     28
   Number with an unused Flip Flop:      14  out of     28    50%
   Number with an unused LUT:             0  out of     28     0%
   Number of fully used LUT-FF pairs:    14  out of     28    50%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                          3
 Number of bonded IOBs:                  3  out of    200     1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
```

Fig.4.4 Device Utilization Summary

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.473ns (Maximum Frequency: 287.915MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 5.486ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_ash'
  Clock period: 3.473ns (frequency: 287.915MHz)
  Total number of paths / destination ports: 166 / 19
-------------------------------------------------------------------------
Delay:               3.473ns (Levels of Logic = 3)
  Source:            tx_acc_6 (FF)
  Destination:       tx_acc_0 (FF)
  Source Clock:      clk_ash rising
  Destination Clock: clk_ash rising
```

Fig. 4.5 Timing Report

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is completely routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	High	User specified more than 95% of inputs	
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with timing simulation r...
Device models	High	Device models are Production	
Overall confidence level	Medium		

Fig.4.6 Confidence Level

Device	
Family	Spartan6
Part	xc6slx9
Package	csg324
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Characterization	
Production	v1.3,2011-05-04

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	25	5720	0
Signals	0.000	30	---	---
IOs	0.000	3	200	2
Leakage	0.014			
Total	0.014			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	30.5	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

Supply Power (W)	Total	Dynamic	Quiescent
	0.014	0.000	0.014

Fig.4.7 Power Report

4.4.2 TRANSMITTER

The transmitter consists of 8 bit din , clken, clk_ash, wr_en as input data . It converts the parallel data to serial and gives to the tx output ,tx_busy is enabled when the data transmission is in active state.

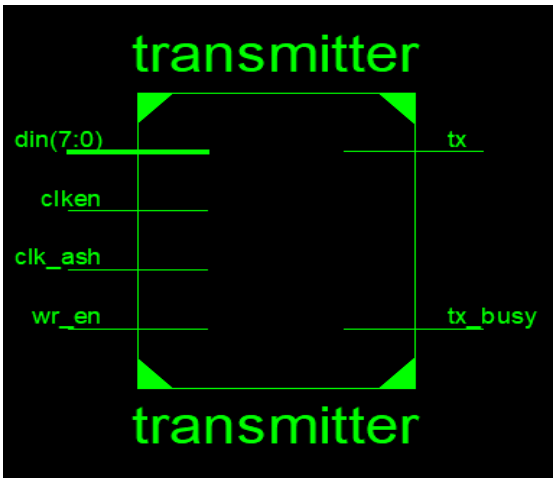


Fig.4.8 RTL Schematic

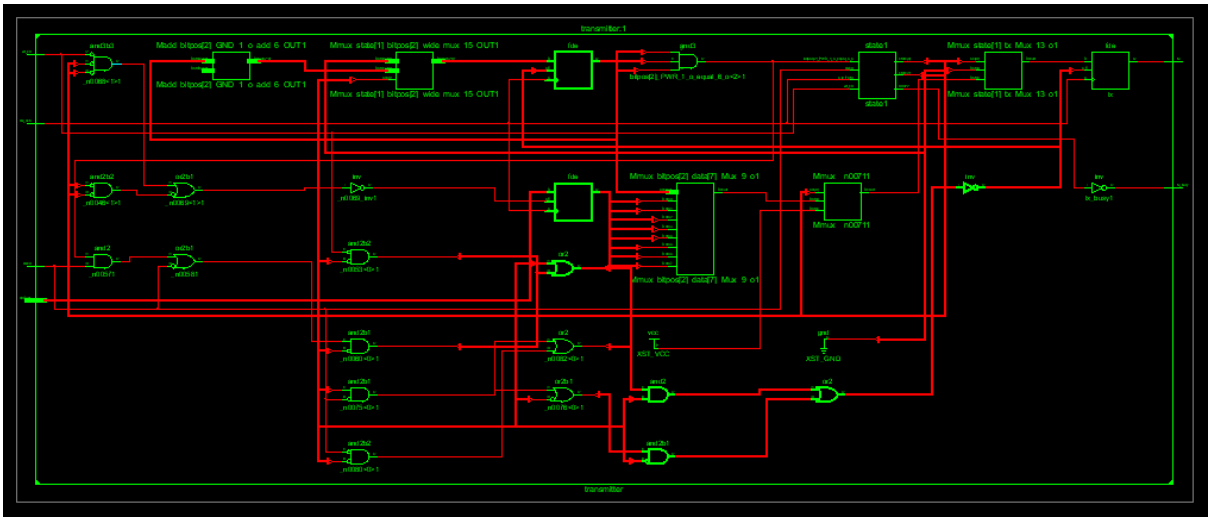


Fig.4.9Expanded RTL Schematic

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
IOs									
wr_en	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
tx_busy	0.00000	LVCMOS25_12_SLOW	0.0	78.1	Async	Async	0	1	0
tx.PAD	0.00000	LVCMOS25_12_SLOW	0.0	35.9	0.0	clk_50m_BUFGP	0	1	0
clken	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
clk_50m	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
din (8)	0.00000	LVCMOS25	0.0	50.0	Async	Async	8	0	0
Total	0.00000					Count	11	2	0

Fig.4.10 I/O Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx9csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              14  out of  11440      0%
 Number of Slice LUTs:                   22  out of   5720      0%
    Number used as Logic:                22  out of   5720      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     22
   Number with an unused Flip Flop:       8  out of     22     36%
   Number with an unused LUT:             0  out of     22      0%
   Number of fully used LUT-FF pairs:    14  out of     22     63%
   Number of unique control sets:         3

IO Utilization:
 Number of IOs:                          13
 Number of bonded IOBs:                  13  out of    200      6%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16      6%
```

Fig.4.11 Device Utilization Summary

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.659ns (Maximum Frequency: 376.102MHz)
   Minimum input arrival time before clock: 3.329ns
   Maximum output required time after clock: 4.852ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_ash'
  Clock period: 2.659ns (frequency: 376.102MHz)
  Total number of paths / destination ports: 69 / 23
-------------------------------------------------------------------------
Delay:               2.659ns (Levels of Logic = 1)
  Source:            state_FSM_FFd1 (FF)
  Destination:       data_0 (FF)
  Source Clock:      clk_ash rising
  Destination Clock: clk_ash rising
```

Fig. 4.12 Timing Report

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is completely routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	High	User specified more than 95% of inputs	
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with timing simulation r...
Device models	High	Device models are Production	
Overall confidence level	Medium		

Fig.4.13 Confidence Level

Device	
Family	Spartan6
Part	xc6slx9
Package	csg324
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Characterization	
Production	v1.3,2011-05-04

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	20	5720	0
Signals	0.000	30	---	---
IOs	0.000	13	200	7
Leakage	0.014			
Total	0.014			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	30.5	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

Fig.4.14 Power Report

4.4.3 RECEIVER

The receiver consists of clken, clk_50m, rdy_clr,rx as input data . It converts the serial data to parallel form and gives to the 8 bit data output ,rdy is enabled when the data is received.

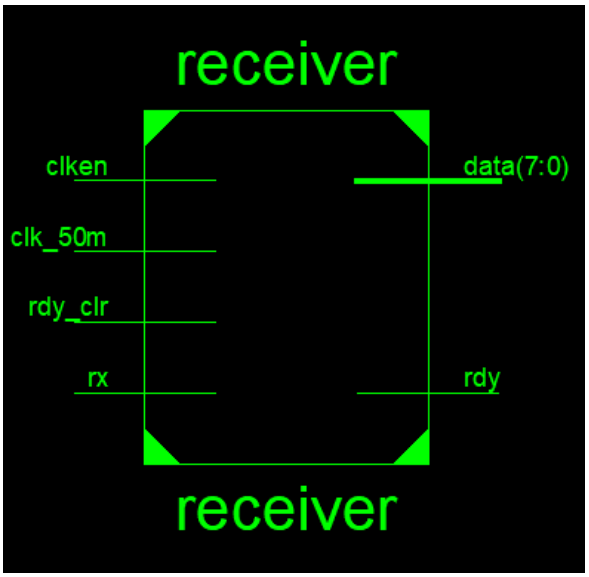


Fig.4.15 RTL Schematic

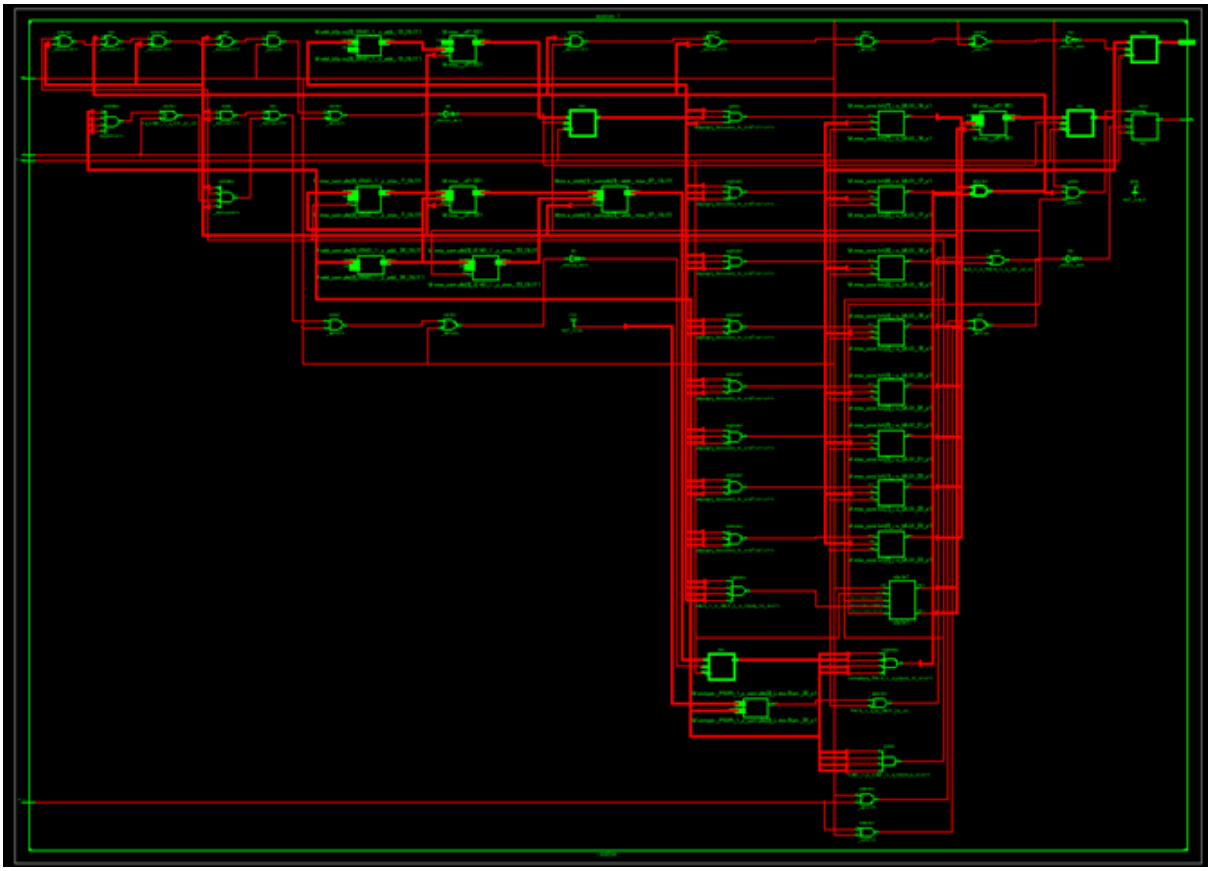


Fig.4.16 Expanded RTL Schematic

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
⊟ IOs									
rx	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
rdy_clr	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
rdy.PAD	0.00000	LVCMOS25_12_SLOW	0.0	27.5	0.0	clk_50m_BUFGP	0	1	0
clken	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
clk_50m	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
⊞ data (8)	0.00000	LVCMOS25_12_SLOW	0.0	50.0	0.0	clk_50m_BUFGP	0	8	0
Total	0.00000					Count	4	9	0

Fig.4.17 I/O Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx9csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              14  out of  11440      0%
 Number of Slice LUTs:                   28  out of   5720      0%
    Number used as Logic:                28  out of   5720      0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     28
   Number with an unused Flip Flop:      14  out of     28     50%
   Number with an unused LUT:             0  out of     28      0%
   Number of fully used LUT-FF pairs:    14  out of     28     50%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                          3
 Number of bonded IOBs:                  3  out of    200      1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16      6%
```

Fig.4.18 Device Utilization Summary

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.005ns (Maximum Frequency: 332.823MHz)
   Minimum input arrival time before clock: 4.077ns
   Maximum output required time after clock: 3.634ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_50m'
  Clock period: 3.005ns (frequency: 332.823MHz)
  Total number of paths / destination ports: 303 / 51
-------------------------------------------------------------------------
Delay:               3.005ns (Levels of Logic = 2)
  Source:            sample_1 (FF)
  Destination:       scratch_0 (FF)
  Source Clock:      clk_50m rising
  Destination Clock: clk_50m rising
```

Fig. 4.19 Timing Report

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is completely routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	High	User specified more than 95% of inputs	
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with timing simulation r...
Device models	High	Device models are Production	
Overall confidence level	Medium		

Fig.4.20 Confidence Level

Device	
Family	Spartan6
Part	xc6slx9
Package	csg324
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Characterization	
Production	v1.3,2011-05-04

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	47	5720	1
Signals	0.000	55	---	---
IOs	0.000	13	200	7
Leakage	0.014			
Total	0.014			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	30.5	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

Fig.4.21 Power Report

4.4.4 TOP MODULE(UART)

The top module consists of all the submodules of Baud rate generation,transmitter and receiver where the input are 8 bit din,clk_50m, rdy_clr ,rx, wr_en as input data and 8bit dout,rdy,tx,tx_busy as output.

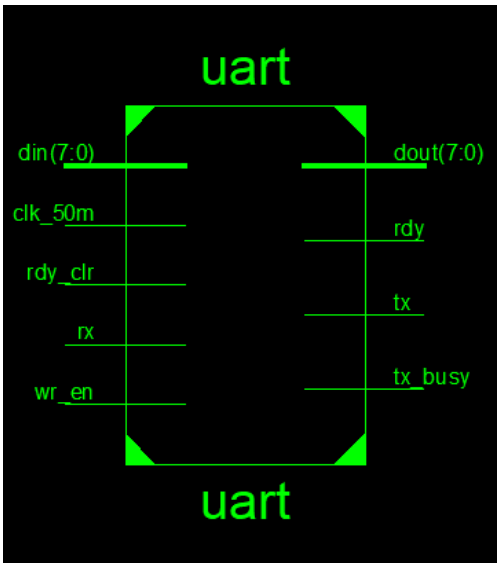


Fig.4.22 RTL Schematic

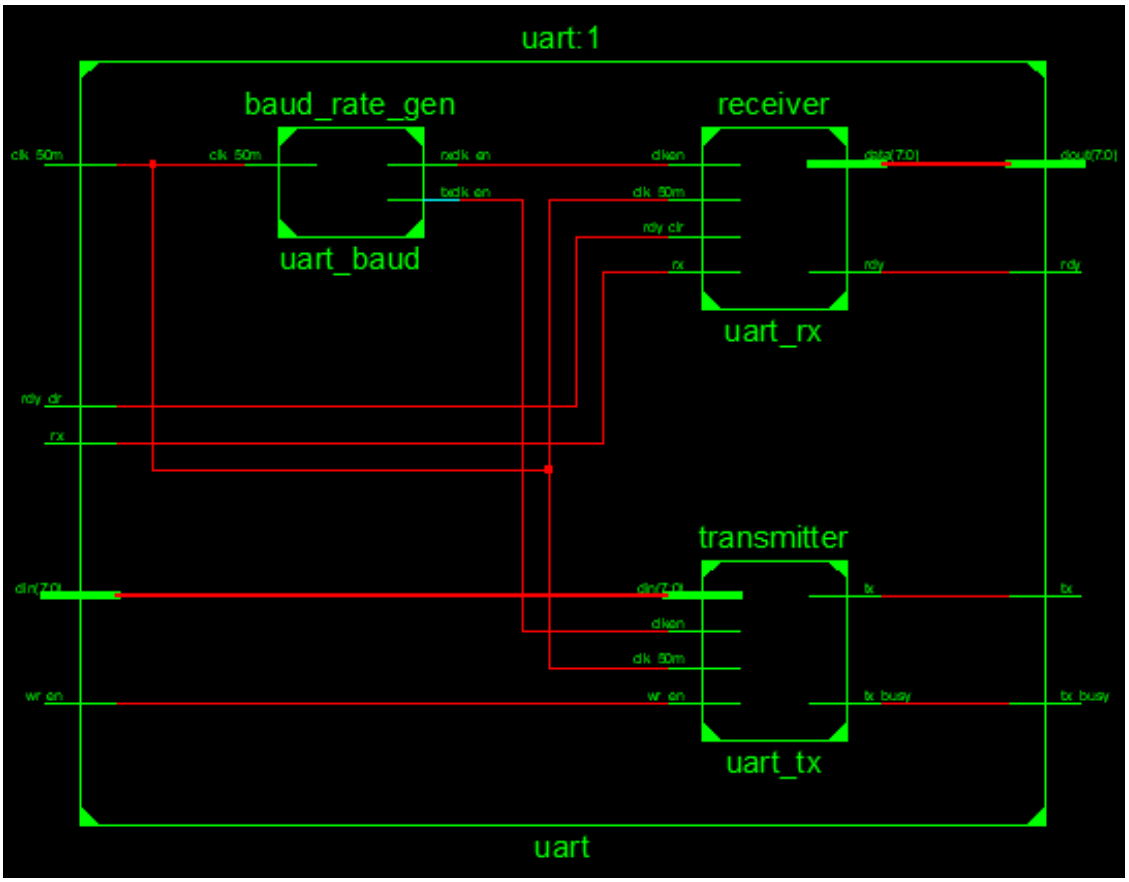


Fig.4.23 Expanded RTL Schematic

Name	Power (W)	I/O Standard	Signal Rate	% High	Clock (MHz)	Clock Name	Input Pins	Output Pins	Bidir Pins
⊟ IOs									
wr_en	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
tx_busy	0.00000	LVCMOS25_12_SLOW	0.0	81.2	Async	Async	0	1	0
tx	0.00000	LVCMOS25_12_SLOW	0.0	50.0	0.0	clk_50m_BUFGP	0	1	0
rx	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
rdy_clr	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
rdy	0.00000	LVCMOS25_12_SLOW	0.0	25.2	0.0	clk_50m_BUFGP	0	1	0
clk_50m	0.00000	LVCMOS25	0.0	50.0	Async	Async	1	0	0
⊞ din (8)	0.00000	LVCMOS25	0.0	50.0	Async	Async	8	0	0
⊞ dout (8)	0.00000	LVCMOS25_12_SLOW	0.0	50.0	0.0	clk_50m_BUFGP	0	8	0
Total	0.00000					Count	12	11	0

Fig.4.24 I/O Report

```
Device utilization summary:
---------------------------

Selected Device : 6slx9csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              55  out of  11440      0%
 Number of Slice LUTs:                   91  out of   5720      1%
    Number used as Logic:                91  out of   5720      1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     97
   Number with an unused Flip Flop:      42  out of     97     43%
   Number with an unused LUT:             6  out of     97      6%
   Number of fully used LUT-FF pairs:    49  out of     97     50%
   Number of unique control sets:         5

IO Utilization:
 Number of IOs:                          23
 Number of bonded IOBs:                  23  out of    200     11%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16      6%
```

Fig.4.25 Device Utilization Summary

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.954ns (Maximum Frequency: 252.940MHz)
   Minimum input arrival time before clock: 4.585ns
   Maximum output required time after clock: 4.825ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk_50m'
  Clock period: 3.954ns (frequency: 252.940MHz)
  Total number of paths / destination ports: 737 / 93
-------------------------------------------------------------------------
Delay:               3.954ns (Levels of Logic = 3)
  Source:            uart_rx/sample_1 (FF)
  Destination:       uart_rx/bitpos_3 (FF)
  Source Clock:      clk_50m rising
  Destination Clock: clk_50m rising
```

Fig. 4.26 Timing Report

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is completely routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	High	User specified more than 95% of inputs	
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with timing simulation r...
Device models	High	Device models are Production	
Overall confidence level	Medium		

Fig.4.27 Confidence Level

Device	
Family	Spartan6
Part	xc6slx9
Package	csg324
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Characterization	
Production	v1.3,2011-05-04

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	78	5720	1
Signals	0.000	111	---	---
IOs	0.000	23	200	12
Leakage	0.014			
Total	0.014			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	30.5	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

Fig.4.28 Power Report

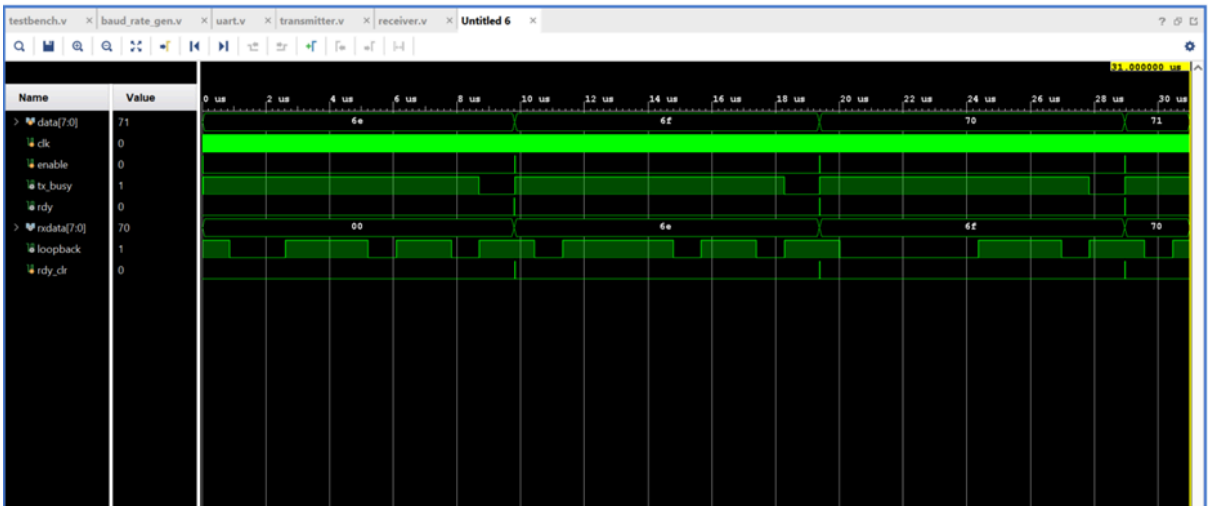


Fig.4.29 Simulation Results

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

This chapter summarizes the work done in this project. It also gives ideas for possible future work directions.

5.1 CONCLUSION

In this project UART design is developed using Verilog and the functionality is verified using Verilog.

5.2 FUTURE SCOPE

Future scope is to verify the functionality Verification of UART using System verilog which allows us to create a much more flexible test environment with reusable components. Further it will also present a verification architecture of configurable Verification IP for UART interface.

CHAPTER 7

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