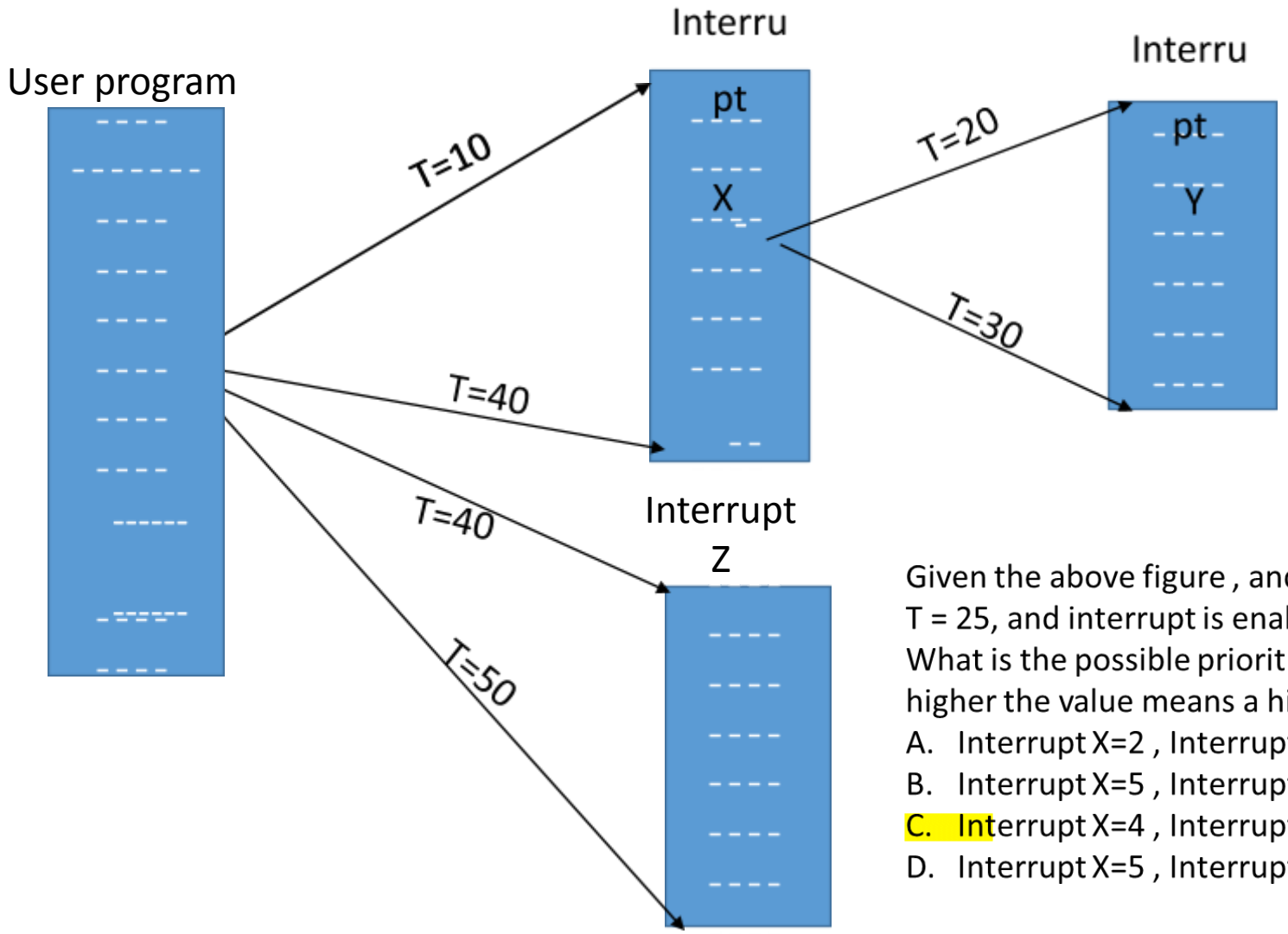


Given the above figure , and if Interrupt Z signal was received at time T = 25, and interrupt is enabled with priority.
What is the possible priorities for each of the three Interrupts(The higher the value means a higher priority):

A. Interrupt X=2 , Interrupt Y =4, Interrupt handler Z = 5
B. Interrupt X=5 , Interrupt Y =4, Interrupt handler Z =2
C. Interrupt X=4 , Interrupt Y =5, Interrupt handler Z = 2
D. Interrupt X=5 , Interrupt Y =2, Interrupt handler Z = 4

Which register in the figure is responsible for storing the address in memory for the next read or write?

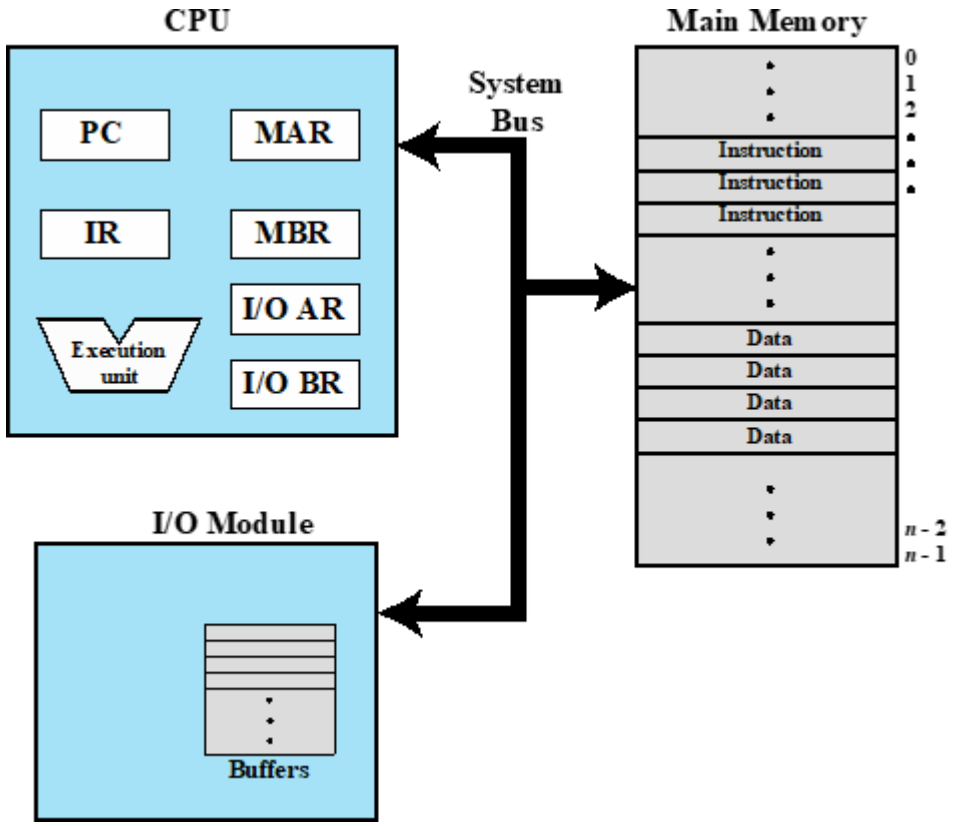
a) PC

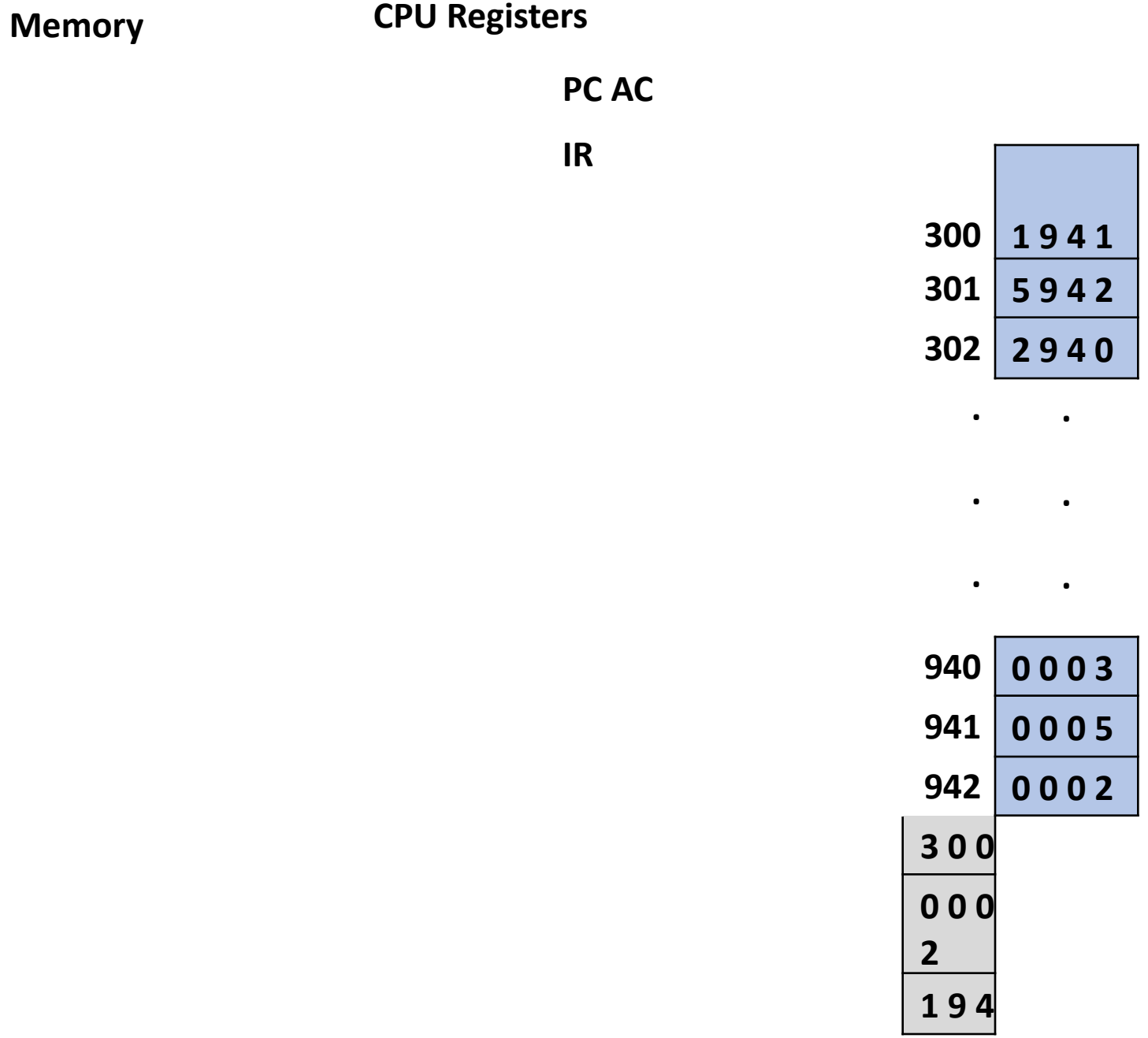
b)IR

c)MAR

d)MBR

e) I/O AR




Memory
CPU Registers
PC AC
IR
300 1 9 4 1
301 5 9 4 2
302 2 9 4 0
940 0 0 0 3
941 0 0 0 5
942 0 0 0 2
3 0 0
0 0 0 2
1 9 4

0

0001 =
Load AC

from
memory
0010 =
Store AC
to

memory
0101 =
Add to AC
from
memory

Given the above figure showing the first fetch instruction.

What is the final result in AC and memory locations 940.

a) 0003

b) 0005

c) 0002

d) [illegible]

e) 0008

Given the figure going from bottom to top which of the following is correct:

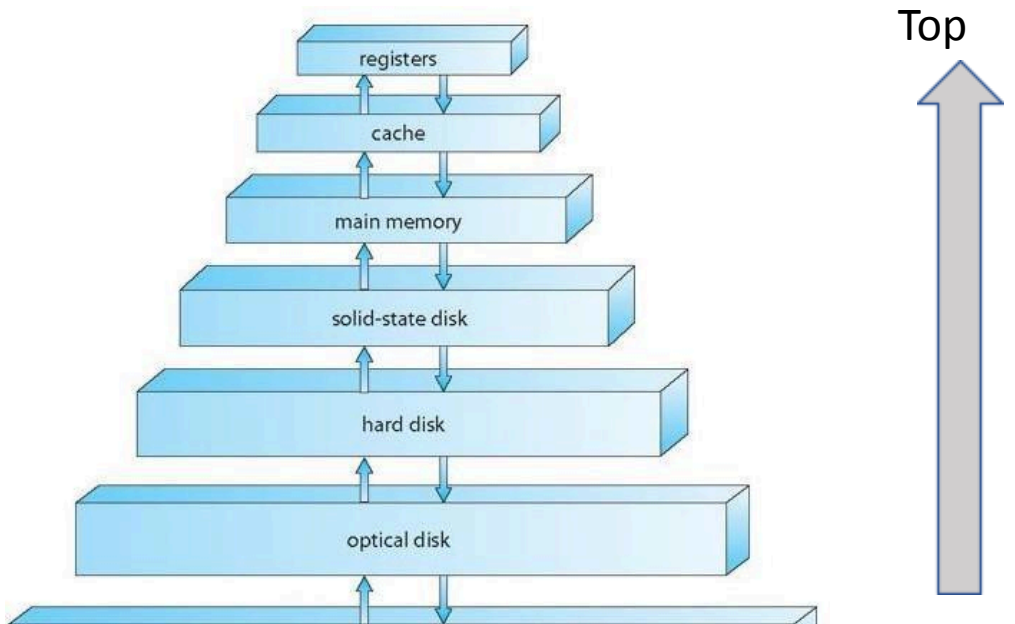
a) Decreasing cost per bit. Increasing capacity. Increasing access time

b) Increasing cost per bit. Decreasing capacity. Increasing access time

c) Increasing cost per bit. Decreasing capacity. Decreasing access time

d) Decreasing cost per bit. Increasing capacity. Decreasing access time

e) Decreasing cost per bit. Decreasing capacity. Decreasing access time



Bottom

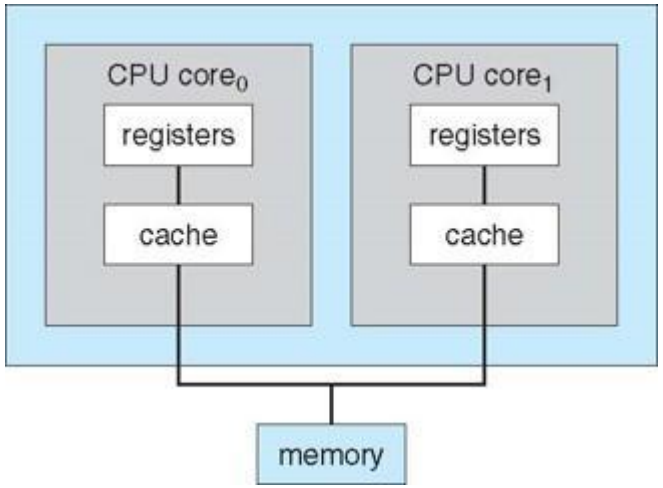
What does the following figure represent:

a) SMP

b) AMP

c) [redacted]

d) DMA



What does A in the figure represent?