```
report_checks -from DFFPOSX1_3/Q -to out1
Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

   Delay      Time   Description
---------------------------------------------------------
    0.00      0.00   clock clk (rise edge)
    1.23      1.23   clock network delay (prop)
    0.16      1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
    0.27      1.66 v DFFPOSX1_3/Q (DFFPOSX1)
    0.08      1.74 v BUFX2_1/Y (BUFX2)
    0.13      1.87 v out1 (out)
              1.87   data arrival time

    1.00      1.00   clock clk (rise edge)
    1.43      2.43   clock network delay (prop)
   -0.25      2.18   Uncertainty
    0.54      2.72   clock reconvergence pessimism
   -2.50      0.22   output external delay
              0.22   data required time
---------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
---------------------------------------------------------
          slack -1.65   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

   Delay      Time   Description
---------------------------------------------------------
    0.00      0.00   clock clk (rise edge)
    1.23      1.23   clock network delay (prop)
    0.16      1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
    0.27      1.66 v DFFPOSX1_3/Q (DFFPOSX1)
    0.08      1.74 v BUFX2_1/Y (BUFX2)
    0.13      1.87 v out1 (out)
              1.87   data arrival time
```

```
   1.00       1.00   clock clk (rise edge)
   1.43       2.43   clock network delay (prop)
  -0.25       2.18   Uncertainty
   0.54       2.72   clock reconvergence pessimism
  -2.50       0.22   output external delay
              0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
          slack -1.43   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

    Delay       Time   Description
-----------------------------------------------------------
   0.00       0.00   clock clk (rise edge)
   1.23       1.23   clock network delay (prop)
   0.16       1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
   0.27       1.66 v DFFPOSX1_3/Q (DFFPOSX1)
   0.08       1.74 v BUFX2_1/Y (BUFX2)
   0.13       1.87 v out1 (out)
              1.87   data arrival time

   1.00       1.00   clock clk (rise edge)
   1.43       2.43   clock network delay (prop)
  -0.25       2.18   Uncertainty
   0.54       2.72   clock reconvergence pessimism
  -2.50       0.22   output external delay
              0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
          slack -1.23   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max
```

```
   Delay      Time   Description
---------------------------------------------------------
   0.00      0.00   clock clk (rise edge)
   1.23      1.23   clock network delay (prop)
   0.16      1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
   0.27      1.66 v DFFPOSX1_3/Q (DFFPOSX1)
   0.08      1.74 v BUFX2_1/Y (BUFX2)
   0.13      1.87 v out1 (out)
             1.87   data arrival time

   1.00      1.00   clock clk (rise edge)
   1.43      2.43   clock network delay (prop)
  -0.25      2.18   Uncertainty
   0.54      2.72   clock reconvergence pessimism
  -2.50      0.22   output external delay
             0.22   data required time
---------------------------------------------------------
             0.22   data required time
            -1.87   data arrival time
---------------------------------------------------------
         slack -1.05   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

   Delay      Time   Description
---------------------------------------------------------
   0.00      0.00   clock clk (rise edge)
   1.23      1.23   clock network delay (prop)
   0.16      1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
   0.27      1.66 v DFFPOSX1_3/Q (DFFPOSX1)
   0.08      1.74 v BUFX2_1/Y (BUFX2)
   0.13      1.87 v out1 (out)
             1.87   data arrival time

   1.00      1.00   clock clk (rise edge)
   1.43      2.43   clock network delay (prop)
  -0.25      2.18   Uncertainty
   0.54      2.72   clock reconvergence pessimism
  -2.50      0.22   output external delay
```

```
              0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
        slack -0.87   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

    Delay      Time   Description
-----------------------------------------------------------
     0.00      0.00   clock clk (rise edge)
     1.23      1.23   clock network delay (prop)
     0.16      1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
     0.27      1.66 v DFFPOSX1_3/Q (DFFPOSX1)
     0.08      1.74 v BUFX2_1/Y (BUFX2)
     0.13      1.87 v out1 (out)
               1.87   data arrival time

     1.00      1.00   clock clk (rise edge)
     1.43      2.43   clock network delay (prop)
    -0.25      2.18   Uncertainty
     0.54      2.72   clock reconvergence pessimism
    -2.50      0.22   output external delay
               0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
        slack -0.72   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

    Delay      Time   Description
-----------------------------------------------------------
     0.00      0.00   clock clk (rise edge)
     1.23      1.23   clock network delay (prop)
```

```
   0.16       1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
   0.27       1.66 v DFFPOSX1_3/Q (DFFPOSX1)
   0.08       1.74 v BUFX2_1/Y (BUFX2)
   0.13       1.87 v out1 (out)
              1.87   data arrival time

   1.00       1.00   clock clk (rise edge)
   1.43       2.43   clock network delay (prop)
  -0.25       2.18   Uncertainty
   0.54       2.72   clock reconvergence pessimism
  -2.50       0.22   output external delay
              0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
          slack -0.65   (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

    Delay       Time   Description
-----------------------------------------------------------
   0.00       0.00   clock clk (rise edge)
   1.23       1.23   clock network delay (prop)
   0.16       1.39 ^ DFFPOSX1_3/CLK (DFFPOSX1)
   0.27       1.66 v DFFPOSX1_3/Q (DFFPOSX1)
   0.08       1.74 v BUFX2_1/Y (BUFX2)
   0.13       1.87 v out1 (out)
              1.87   data arrival time

   1.00       1.00   clock clk (rise edge)
   1.43       2.43   clock network delay (prop)
  -0.25       2.18   Uncertainty
   0.54       2.72   clock reconvergence pessimism
  -2.50       0.22   output external delay
              0.22   data required time
-----------------------------------------------------------
              0.22   data required time
             -1.87   data arrival time
-----------------------------------------------------------
```

slack -0.49 (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

Delay	Time	Description
0.00	0.00	clock clk (rise edge)
1.23	1.23	clock network delay (prop)
0.16	1.39	^ DFFPOSX1_3/CLK (DFFPOSX1)
0.27	1.66	v DFFPOSX1_3/Q (DFFPOSX1)
0.08	1.74	v BUFX2_1/Y (BUFX2)
0.13	1.87	v out1 (out)
	1.87	data arrival time
1.00	1.00	clock clk (rise edge)
1.43	2.43	clock network delay (prop)
-0.25	2.18	Uncertainty
0.54	2.72	clock reconvergence pessimism
-2.50	0.22	output external delay
	0.22	data required time
	0.22	data required time
	-1.87	data arrival time

slack -0.41 (VIOLATED)

Startpoint: DFFPOSX1_3 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: reg-to-out
Path Type: max

Delay	Time	Description
0.00	0.00	clock clk (rise edge)
1.23	1.23	clock network delay (prop)
0.16	1.39	^ DFFPOSX1_3/CLK (DFFPOSX1)
0.27	1.66	v DFFPOSX1_3/Q (DFFPOSX1)
0.08	1.74	v BUFX2_1/Y (BUFX2)
0.13	1.87	v out1 (out) 9310101068-
	1.87	data arrival time

```
      1.00       1.00   clock clk (rise edge)
      1.43       2.43   clock network delay (prop)
     -0.25       2.18   Uncertainty
      0.54       2.72   clock reconvergence pessimism
     -2.50       0.22   output external delay
                 0.22   data required time
-----------------------------------------------------------
                 0.22   data required time
                -1.87   data arrival time
-----------------------------------------------------------
            slack -0.33   (VIOLATED)
```