16 Channel - 24 Bit ADC module

(9B)

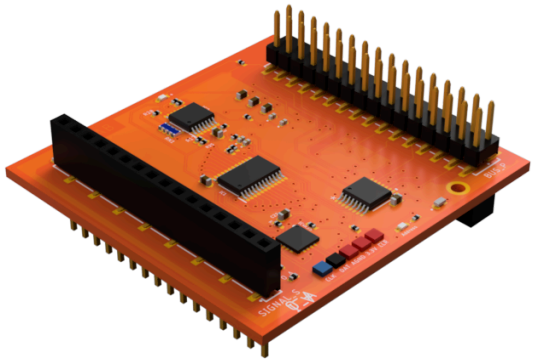

Fig 1: 16 Channel 24 Bit ADC Module

The 16 channel 24 bit ADC module used in various applications like:

- Voice sampling
- Strain gauges
- Low voltage sensing

The Single ADC has an inbuilt 24 bit ADC with a maximum sampling rate of 32kSPS. The board also consists of a 1:16 analog mux. The module converts the single ended inputs to differential inputs to improve linearity and noise performance. The MUX allows access to input pins (I1 to I16) of the E-LAGORi board..

Include the library ELi_SaM_7_00.h in order to use these boards.

(Github:https://github.com/E-Lagori/ELi_SaM_7_00)

Default address is 0x81. Maximum mux switching speed is 432Hz.
RMS error : 0.6618%

The block diagram of 16 Channel 24 Bit ADC Module is as shown in fig 2:

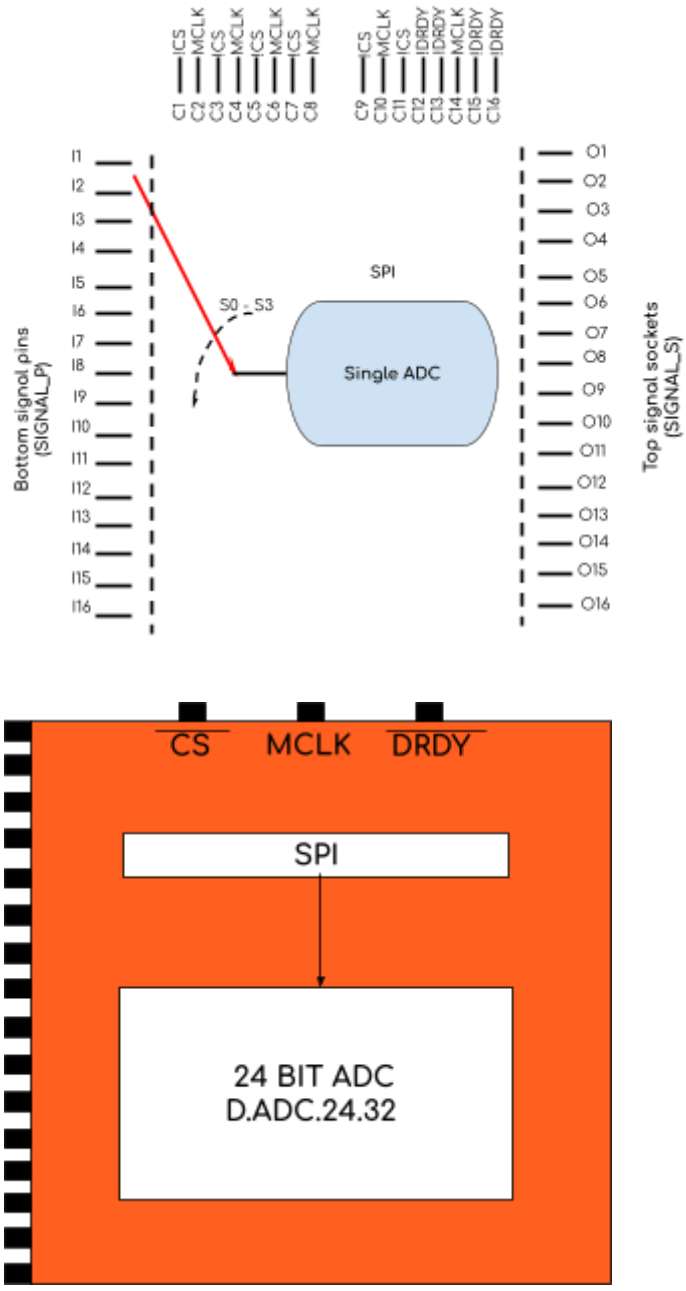

Fig. 2: Block diagram

The 24-Bit 16 channel ADC module linearity graph is as shown in Fig 3.

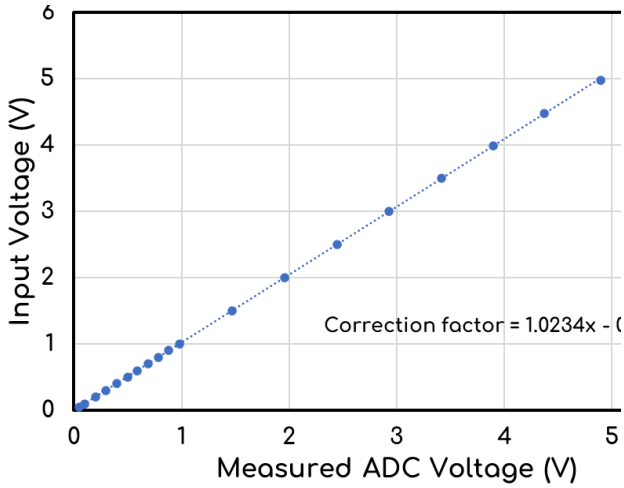

Fig 3: Typical graph of measured ADC voltage vs input voltage

The pin details and configuration are listed as in the table below.

SIGNAL_P

Jumper	Description
I1	Channel 0 of MUX to ADC
I2	Channel 1 of MUX to ADC
I3	Channel 2 of MUX to ADC
I4	Channel 3 of MUX to ADC
I5	Channel 4 of MUX to ADC
I6	Channel 5 of MUX to ADC
I7	Channel 6 of MUX to ADC
I8	Channel 7 of MUX to ADC
I9	Channel 8 of MUX to ADC
I10	Channel 9 of MUX to ADC
I11	Channel 10 of MUX to ADC
I12	Channel 11 of MUX to ADC
I13	Channel 12 of MUX to ADC
I14	Channel 13 of MUX to ADC
I15	Channel 14 of MUX to ADC
I16	Channel 15 of MUX to ADC

BUS_S/BUS_P

Jumper	Description
C1	CS (Active low)
C2	Master Clock (MCLK)
C3	CS (Active low)
C4	Master Clock (MCLK)
C5	CS (Active low)
C6	Master Clock (MCLK)
C7	CS (Active low)
C8	Master Clock (MCLK)
C9	CS (Active low)
C10	Master Clock (MCLK)
C11	CS (Active low)
C12	Data ready (High - Low)
C13	Data ready (High - Low)
C14	Master Clock (MCLK)
C15	Data ready (High - Low)
C16	Data ready (High - Low)