I – SEMESTER (F)

CMOS VLSI DESIGN

Subject Code	: **10EC021**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

CMOS Process Technology: Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques

CMOS Analog Design: Introduction, Single Amplifier. Differential

Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.

REFERENCE BOOKS:

1. Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspective**," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
2. Wayne, Wolf, "**Modern VLSI design: System on Silicon" Pearson Education**", Second Edition
3. Douglas A Pucknell & Kamran Eshragian , "**Basic VLSI Design**" PHI 3rd Edition (original Edition – 1994)
4. Sung Mo Kang & Yosuf Lederabic Law, "**CMOS Digital Integrated Circuits: Analysis and Design**", McGraw-Hill (Third Edition)

VLSI Design Verification

Subject Code	: **10EC046**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Today, the complexity of the VLSI integrated circuits that are being designed is so large that pre-silicon verification presents a major challenge to the design team. The fact that IP from multiple sources are integrated today to create a system-on-chip design further complicates the matter. Simulation based verification techniques that were developed in the past are considered inadequate to-day, since they require too many test cases and require too much development time and run-time. Raising the level of abstraction to design can help bring down the simulation cost. Formal specification and verification techniques are another way to address the challenge of design verification.

Importance of Design Verification: In the SoC Design context. SoC Design flow and the role of Design Verification in the flow. Difference between verification, testing, and post-silicon validation. Why is pre-silicon verification required? Types of Design Verification - Functional Verification, Performance Verification. Simulation, Emulation, Formal and Semi-formal verification.

System-level Verification: System-level test benches and their merits. Applying system-level test benches, Emulation, hardware acceleration.

Block-level Veriifcation. Functional Verification through simulation. Whitebox, blockbox and Graybox testing. Coverage Metrics and code coverage analysis. Creating testbenches in Verilog/.VHDL Programming Language Interfaces (PLI). Formal checking of blocks – linting and formal model checking. Examples.

Design Representation: Creating hardware models. Verilog and VHDL models. SPICE models for Analog circuits.

Analog and Mixed-Signal Verification. Using SPICE for simulation.

Simulation: Event based and cycle based simulation. Speeding up of simulation through hardware accelerators. Rigid Prototyping. FPGA as Logic Emulators.

Static Timing Verification. Concept of static timing analysis. Timing constraints, timing models, critical path analysis, false paths.

Physical Design Verification. Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, cross talk and reliability checks.

IP-Reuse in modern-day SoC. SoC Integration and the problem of verification of IP-based designs. Verification IP and their importance.

Formal Verification: Techniques for FSM Models: Models Checking and Formal Engines. SAT Solvers, BDDs, Symbolic Model Checking with BDDs, Model Checking using SAT, Equivalence Checking.

Reference Books:

1. Prakash Rashinkar, Peter Paterson and Leena Singh **"System – on – a - Chip Verification – Methodology and Techniques**" , Kulwer Publishers, 2001.
2. "An excellent source for instructors for Formal Verification techniques" (website developed by) Prof. V. Narayanan, Penn State University, USA. http://www.cse.psu.edu/~vijay/verify/instuctors.html
3. S. Minato " **Binary Decision Diagram and Applications for VLSI CAD**", Kulwer Academic Pub. November 1996.
4. Edmund M Clarke, O. Grumberg & D. Long "**Model Checking**",.

Conference Proceedings:

1. DVCON – Design Verification Conference is exclusively devoted to the topic of Design Verification.
2. Design Automation Conference (DAC)
3. International Conferences on Computer Aided Design (ICCAD)
4. Formal Methods in Computer Aided Design (FMCAD)
5. Computer Aided Verification (CAV).

SoC Design

Subject Code	: 10EC0xx	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Goal of the course – Today, VLSI chips are entire "system-on-chip" designs, which include processors, memories, peripheral controllers, and connectivity sub-systems. The course aims to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow.

Motivation for SoC Design - Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

Embedded Processors – microprocessors, microcontrollers, DSP and their selection criteria. Review of RISC and CISC instruction sets, Von-Neumann and Harward architectures, and interrupt architectures.

Embedded Memories – scratchpad memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

Hardware Accelerators in an SOC – comparison on hardware accelerators and general-purpose CPU. Accelerators for graphics and image processing. Typical peripherals in an SoC – DMA controller, USB controller.

Interconnect architectures for SoC. Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.

Mixed Signal and RF components in an SoC. Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits.

SoC Design Flow. IP design, verification and integration, hardware-software codesign, power management problems, and packaging related problems.

Reference Books

1. Sudeep Pasricha and Nikil Dutt,"On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008
2. Henry Chang et al., "Surviving the SOC revolution: a guide to platform-based design", Kluwer (Springer), 1999
3. Frank Ghenassia,"Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems", Springer © 2005 (281 pages), ISBN:9780387262321
4. Luca Benini and Giovanni De Micheli,"Networks on Chips: Technology and Tools", Morgan Kaufmann Publishers © 2006 (408 pages), ISBN:9780123705211,

EMBEDDED SYSTEM DESIGN

Subject Code	: **10EC037**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Typical Embedded System : Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components Characteristics and Quality Attributes of Embedded Systems

Hardware Software Co-Design and Program Modelling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modelling Language, Hardware Software Trade-offs

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages Real-Time Operating System (RTOS) based Embedded System Design.

Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Trends in the Embedded Industry : Processor Trends in Embedded System, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.

Reference Books:

1. **Introduction to Embedded Systems,** Shibu K V, Tata McGraw Hill Education Private Limited, 2009
2. **Embedded Systems – A contemporary Design Tool**, James K Peckol, John Weily, 2008.

REFERENCE BOOKS:

1. K V Shibu, " Introduction to Embedded Systems", TMH 2009 (modify the contents - by N Udupa)
2. Raj Kamal, "**Embedded systems Architecture, Programming and Design**", TMH.
3. J. W. Valvano, "**Embedded Microcomputer system – Real time Interfacing**", Thomson Learning Publishing
4. Jane W. S., Liu, "**Real Time Systems**", Pearson Education Asia Pub

ELECTIVE – I

DIGITAL SYSTEM DESIGN USING VERILOG

Subject Code	: **10EC0xx**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction and Methodology:
Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.

Combinational Basics:
Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

Number Basics:
Unsigned and Signed Integers, Fixed and Floating-point Numbers.

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.

Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test,

Refernces:

1. "**Digital Design: An Embedded Sytems Approach Using VERILOG",** Peter J. Ashenden, Elesvier, 2010.

NANOELECTRONICS

Subject Code	: **10EC054**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Shrink-down Approaches: Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.), Resonant Tunneling Transistors, Single electron transistors, new storage, optoelectronic, and spintronics devices.

Atoms-up Approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics, molecular interconnects; Carbon nanotube electronics, band structure & transport, devices, applications.

REFERENCE BOOKS:

1. C.P. Poole Jr., F.J. Owens, "**Introduction to Nanotechnology**", Wiley (2003).
2. Waser Ranier, "**Nanoelectronics and Information Technology**" (Advanced Electronic Materials and Novel Devices), Wiley-VCH (2003)
3. K.E. Drexler, "**Nano systems**", Wiley (1992)

4. John H. Davies, "**The Physics of Low-Dimensional Semiconductors**", Cambridge University Press, 1998
Research Papers

ASIC DESIGN

Subject Cod	: **10EC012**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Note All Designs Will Be Based On VHDL

Introduction: Full Custom with ASIC, Semi custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries
Data Logic Cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

ASIC Library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

Low-Level Design Entry: Schematic Entry: Hierarchical design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation

Programmable ASIC: programmable ASIC logic cell, ASIC I/O cell

A Brief Introduction to Low Level Design Language: an introduction to EDIF, PLA Tools, an introduction to CFI designs representation. Half gate ASIC. Introduction to Synthesis and Simulation;

ASIC Construction Floor Planning and Placement And Routing: Physical Design, CAD Tools, System Partitioning, Estimating ASIC size, partitioning methods. Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time

driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

EFERENCE BOOKS:

1. M.J.S .Smith, - "**Application - Specific Integrated Circuits**" – Pearson Education, 2003.
2. Jose E.France, Yannis Tsividis, "**Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing**", Prentice Hall, 1994.
3. Malcolm R.Haskard; Lan. C. May, "**Analog VLSI Design - NMOS and CMOS**", Prentice Hall, 1998.
4. Mohammed Ismail and Terri Fiez, "**Analog VLSI Signal and Information Processing"**, McGraw Hill, 1994.

1. II – SEMESTER

DESIGN OF ANALOG & MIXED MODE VLSI CIRCUITS

Subject Code	: **10EC025**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.

Single stage Amplifier: CS stage with resistance load, divide connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascade stage, choice of device models.

Differential Amplifiers: Basic difference pair, common mode

response, Differential pair with MOS loads, Gilbert cell.

Passive and active Current mirrors: Basic current mirrors, Cascade mirrors, active current mirrors.

Frequency response of CS stage: source follower, Common gate stage, Cascade stage and Difference pair. Noise in CS stage, C- G stage, source follower, cascade stage, differential pair.

Operational Amplifiers: One Stage OP-Amp. Two Stage OP-Amp, Gain boosting, Coommon Mode Feedback, Slew rate, PSRR. Compenastion of 2stage OP-Amp, Other compensation techniques.

Oscillators: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO.

PLL: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Bandgap Refernces and Switched capacitor filetrs.

References:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH, 2007.

1. REAL TIME OPERATING SYSTEMS

Subject Code	: **10EC0xx**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Esecutive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant

Functions.

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.

I/O Resources:
Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.
Memory:
Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems.

Multiresource Services:
Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:
Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Embedded System Components:
Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:
Execptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

Performance Tuning:
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

High availability and Reliability Design:
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. **(Chap 13 of book Myke Predko)**

References:

1. "**Real-Time Embedded Systems and Components" ,** Sam Siewert, Cengage Learning India Edition, 2007.
2. " **Programming and Customizing the PIC microcontroller" ,** Myke Predko, 3rd Ed, TMH, 2008

ADVANCED MICROCONTROLLERS

Subject Code	: **10EC0xx**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Microcontrollers have become prevalent in a number of applications such as instrumentation, industrial electronics, automotive electronics, robotics, etc. Advances in VLSI technology permit the integration of not only the processor but also the analog electronics, memory and peripherals necessary for system implementation; this allows low-cost system implementation. Some microcontrollers used in industrial electronics also provide some digital signal processing capability to further reduce the system cost.
Power dissipation is often a consideration in many systems and modern microcontrollers address it through the support of several low-power modes of operation. The aim of the course is to introduce advanced microcontrollers (16-bit and 32-bit).

Motivation for advanced microcontrollers – Low Power embedded systems, On-chip peripherals, low-power RF capabilities. Examples of applications.

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus –architecture. The assembly language and 'C' programming for MSP-430 microcontrollers. On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock

request feature, Low-power programming and interrupts.

ARM -32 bit Microcontroller family. Architecture of ARM Cortex M3 – General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Register,. Nested Vector Interrupt Controller. Interrupt behavior of ARM Cortex M3. Exceptions Programming. Advanced Programming Features. Memory Protection. Debug Architecture.

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies.

References Books:

1. Joseph Yiu " **The Definitive Guide to the ARM Cortex-M3,** , Newnes, (Elsevier), 2008.
2. John Davies, " **MSP430 Microcontorller Basics**", Newnes (Elsevier Science), 2008.
3. **MSP430 Teaching CD-ROM**, Texas Instruments, 2008.
4. **Sample Programs for MSP430** downloadable from msp430.com
5. David Patterson and John L. Henessay, "**Computer Organization and Design**", (ARM Edition), Morgan Kauffman.

LOW POWER VLSI DESIGN

Subject Code	: **10EC047**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

REFERENCE BOOKS:

1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**" Wiley, 2000
2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002
3. Rabaey, Pedram, "**Low Power Design Methodologies**" Kluwer Academic, 1997

1. ELECTIVE –II

DESIGN OF VLSI SYSTEMS

Subject Code	: **10EC027**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

VLSI System Design Methodology: Structure Design, Strategy, Hierarchy, Regularity, Modularity, and Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design.

Chip Design Methods: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System

Design Capture Tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

Data Path Sub System Design: Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations

Array Subsystem Design: SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays.

Control Unit Design: Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.

Special Purpose Subsystems: Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits, etc

Design Economics: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power, example

VLSI System Testing & Verification: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan

2.

3. **VLSI Applications: Case Study: RISC microcontroller, ATM Switch, etc.**

REFERENCE BOOKS:

1. Neil H.E. Weste, Davir Harris, "**CMOS VLSI Design: A Circuits and System Perspectives**" Addison Wesley - Pearson Education, 3rd Edition, 2004.
2. Wayne, Wolf, "**Modern VLSI Design: System on Silicon**" Prentice Hall PTR/Pearson Education, Second Edition, 1998
3. Douglas A Pucknell & Kamran Eshragian , "**Basic VLSI Design**" PHI 3rd Edition (original Edition – 1994)

VLSI DESIGN AUTOMATION

Subject Code	: **10EC010**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

4. **Logic Synthesis & Verification:** Introduction to combinational logic synthesis, Binary Decision Diagram, Hardware models for High-level synthesis.

VLSI Automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms

Placement, Floor Planning & Pin Assignment: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment

Global Routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches

Detailed Routing: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms

Over The Cell Routing & Via Minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction

REFERENCE BOOKS:

1. Naveed Shervani, "**Algorithms for VLSI physical design Automation**", Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, "**Algorithm and Data Structures for VLSI Design**", KAP, 2002.
3. Rolf Drechsheler : "**Evolutionary Algorithm for VLSI**", Second edition
4. Trimburger, "**Introduction to CAD for VLSI**", Kluwer Academic publisher, 2002

MODERN DSP

Subject Code	: **10EC0xx**	IA Marks	: 50
No. of Lecture Hours/Week	: 04	Exam Marks	: 03
Total No. of Lecture Hours	: 52	Exam Hours	: 100

Goal of the course – Advances in Digital Signal Processing involve variable sampling rates and thus the multirate signal processing and hence their applications in communication systems and signal processing. It is intended to introduce a basic course in multirate signal processing especially meant for students of branches eligible for M Tech courses in EC related disciplines.

Review of Signals and Systems – Discrete time processing of continuous signals - Structure of a digital filter; Frequency domain analysis of a digital filter; Quantization error; Sigma and Sigma Delta Modulation. Fourier Analysis – DFT, DTFT, DFT as an estimate of the DTFT for Spectral estimation. DFT for convolution, DFT/DCT for compression, FFT. Ideal Vs non ideal filters, FIR and IIR Filters Digital Filter Implementation; Elementary Operations.

Digital Filters –, State Space realization, Robust implementation of Digital Filters, Robust implementation of equi – ripple FIR digital filters

Multirate Systems and Signal Processing. Fundamentals – Problems and definitions; Upsampling and downsampling; Sampling rate conversion by a rational factor;

Multistage implementation of digital filters; Efficient implementation of multirate systems.

DFT filter banks and Transmultiplexers – DFT filter banks, Maximally Decimated DFT filter banks and Transmultiplexers. Application of transmultiplexers in communications Modulation.

Maximally Decimated Filter banks – Vector spaces, Two Channel Perfect Reconstruction conditions; Design of PR filters Lattice Implementations of Orthonormal Filter Banks, Applications of Maximally Decimated filter banks to an audio signal.

Introduction to Time Frequency Expansion; The STFT; The Gabor Transform, The Wavelet Transform; The Wavelet transform; Recursive Multiresolution Decomposition.

References:

1. Roberto Cristi, "**Modern Digital Signal Processing**", Cengage

Publishers, India, (erstwhile Thompson Publications), 2003.
2. S.K. Mitra, "**Digital Signal Processing: A Computer Based Approach"**, III Ed, Tata McGraw Hill, India, 2007.
3. E.C. Ifeachor and B W Jarvis, "**Digital Signal Processing, a practitioners approach**," II Edition, Pearson Education, India, 2002 Reprint.
4. Proakis and Manolakis, "**Digital Signal Processing**", Prentice Hall 1996 (third edition).

III – SEMESTER

CMOS RF CIRCUIT DESIGN

Subject Code	: **10EC020**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion

RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters

5.

6. **RF Testing:** RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

7.

8. **BJT and MOSFET Behavior at RF Frequencies:** BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

9.

10. **RF Circuits Design:** Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

REFERENCE BOOKS:

1. B. Razavi, "**RF Microelectronics**" PHI 1998
2. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
3. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
4. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

1.
2.
3. ELECTIVE - III

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Subject Code	: **10EC077**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization.

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Two Level Combinational Logic Optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic

minimization, symbolic minimization and encoding property, minimization of Boolean relations.

Multiple Level Combinational Optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization.

Sequential Circuit Optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

Cell Library Binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

Testing: Simulation, Types of simulators, basic components of a simulator, fault simulation Techniques, Automatic test pattern generation methods (ATPG), design for Testability (DFT) Techniques.

REFERENCE BOOKS:

1. Giovanni De Micheli, "**Synthesis and Optimization of Digital Circuits**", Tata McGraw-Hill, 2003.
2. Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, "**Logic Synthesis**", McGraw-Hill, USA, 1994.
3. Neil Weste and K. Eshragian, "**Principles of CMOS VLSI Design: A System Perspective**," 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
4. Kevin Skahill, "**VHDL for Programmable Logic**," Pearson Education (Asia) Pvt. Ltd., 2000.

IMAGE AND VIDEO PROCESSING

Subject Code	: **10EC043**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Introduction: 2D systems, Mathematical preliminaries – Fourier Transform, Z Transform, Optical & Modulation transfer function, Matrix theory, Random signals, Discrete Random fields, Spectral density function.

Image Perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision.

Image Sampling and Quantization: Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization.

Image Transforms: Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, DFT, DCT, DST, Hadamard, Haar, Slant, KLT, SVD transform.

Image Representation by Stochastic Models: Introduction, one-dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions.

Image Enhancement: Point operations, Histogram modeling, spatial operations, Transform operations, Multi-spectral image enhancement, false color and Pseudo-color, Color Image enhancement.

Image Filtering & Restoration: Image observation models, Inverse & Wiener filtering, Fourier Domain filters, Smoothing splines and interpolation, Least squares filters, generalized inverse, SVD and Iterative methods, Maximum entropy restoration, Bayesian methods, Coordinate transformation & geometric correction, Blind de-convolution.

Image Analysis & Computer Vision: Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features,

Texture, Scene matching & detection, Image segmentation, Classification Techniques.

Image Reconstruction from Projections: Introduction, Radon Transform, Back projection operator, Projection theorem, Inverse Radon transform, Fourier reconstruction, Fan beam reconstruction, 3D tomography.

Image Data Compression: Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards.

Video Processing: Fundamental Concepts in Video – Types of video signals, Analog video, Digital video, Color models in video, Video Compression Techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing.

REFERENCE BOOKS:

1. K. Jain**,** "**Fundamentals of Digital Image Processing**," Pearson Education (Asia) Pte. Ltd./Prentice Hall of India, 2004.
2. Z. Li and M.S. Drew**, "Fundamentals of Multimedia**," Pearson Education (Asia) Pte. Ltd., 2004.
3. R. C. Gonzalez and R. E. Woods, "**Digital Image Processing**," 2nd edition, Pearson Education (Asia) Pte. Ltd/Prentice Hall of India, 2004.
4. M. Tekalp, "**Digital Video Processing**," Prentice Hall, USA, 1995.

AUTOMOTIVE ELECTRONICS

Subject Code	:**10EC0xx**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

UNIT 1

Automotive Fundamentals Overview – Four Stroke Cycle, Engine Control, Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Drive Train, Transmission, Brakes, Steering System, Battery, Starting System

UNIT 2

Air/Fuel Systems – Fuel Handling, Air Intake System, Air/ Fuel Management
Sensors – Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Manifold Absolute Pressure (MAP) Sensor - Strain gauge and Capacitor capsule, Engine Coolant Temperature (ECT) Sensor, Intake Air Temperature (IAT) Sensor, Knock Sensor, Airflow rate sensor, Throttle angle sensor
Actuators – Fuel Metering Actuator, Fuel Injector, Ignition Actuator
Exhaust After-Treatment Systems – AIR, Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems

UNIT 3

Electronic Engine Control – Engine parameters, variables, Engine Performance terms, Electronic Fuel Control System, Electronic Ignition control, Idle sped control, EGR Control
Communication – Serial Data, Communication Systems, Protection, Body and Chassis Electrical Systems, Remote Keyless Entry, GPS

UNIT 4

Vehicle Motion Control – Cruise Control, Chassis, Power Brakes, Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension
Automotive Instrumentation – Sampling, Measurement & Signal Conversion of various parameters.

UNIT 5

Integrated Body – Climate Control Systems, Electronic HVAC Systems,

Safety Systems – SIR, Interior Safety, Lighting, Entertainment Systems **Automotive Diagnostics** – Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems

Future Automotive Electronic Systems – Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation, Advance Driver Information System

References: -

1. **William B. Ribbens:** Understanding Automotive Electronics, 6th Edition, SAMS/Elsevier Publishing

2. **Robert Bosch GmbH:** Automotive Electrics Automotive Electronics Systems and Components, 5th edition, John Wiley& Sons Ltd., 2007

4. ELECTIVE-IV

RF AND MICROWAVE CIRCUIT DESIGN

Subject Code	: **10EC071**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks

Passive Circuit Design: The Smith Chart, Application of the Smith Chart in Distributed and lumped element circuit applications, Design of Matching networks.

Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.

Active Networks: Linear and Nonlinear Design: RF/MW Amplifiers Small Signal Design, Large Signal Design, RF/MW Oscillator Design, RF/MW Frequency Conversion Rectifier and Detector Design, Mixer Design, RF/MW Control Circuit Design, RF/MW Integrated circuit design.

Reference BOOKs:

1. Matthew M. Radmanesh**,** "**Radio Frequency and Microwave Electronics Illustrated,**" Pearson Education (Asia) Pte. Ltd., 2004.
2. Reinhold Ludwig and Pavel Bretchko, "**RF Circuit Design: Theory and Applications**," Pearson Education (Asia) Pte. Ltd., 2004.

ADVANCES IN VLSI DESIGN

Subject Code	: **10EC009**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03

Total no. of Lecture Hours	: 52	Exam Marks	: 100

Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.

MESFETS: MESFET and MODFET operations, quantitative description of MESFETS.

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic .Defect tolerant computing,

Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

REFERENCE BOOKS:

1. Kevin F Brrnnan "**Introduction to Semi Conductor Device**", Cambridge publications

2. Eugene D Fabricius "**Introduction to VLSI Design**", McGraw-Hill International publications
3. D.A Pucknell "**Basic VLSI Design**", PHI Publication
4. Wayne Wolf, "**Modern VLSI Design**" Pearson Education, Second Edition , 2002

1.

RF MEMS

Subject Code	: **10EC0xx**	IA Marks	: 50
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

Review – Introduction to MEMS. Fabrication for MEMS, MEMS transducers and Actuators . Microsensing for MEMS, Materials for MEMS. **MEMS materials and fabrication techniques** – Metals, Semiconductors, thin films, Materials for Polymer MEMS, Bulk Machining for silicon based MEMS, Surface machining for Silicon based MEMS, Micro Stereo Lithography for Polymer MEMS.

RF MEMS Switches and micro – relays. Switch Parameters, Basics of Switching, Switches for RF and microwave Applications , Actuation mechanisms, micro relays and micro actuators, Dynamics of Switch operation, MEMS Switch Design and design considerations. MEMS Inductors and capacitors.

Micromachined RF Filters and Phase shifters. RF Filters, Modeling of Mechanical Filters, Micromachanical Filters, SAW filters – Basics, Design considerations. Bulk Acoustic Wave Filters, Micromachined Filters for Millimeter Wave frequencies. Micromacbined Phase Shifters, Types and Limitations, MEMS and Ferroelectric Phase shifters, Applications.

Micromachined transmission lines and components. Micromachined Transmission Lines – Losses in Transmission lines, coplanar lines, Meicroshield and membrane supported lines, Microshield components, Micromachined waveguides, directional couplers and mixers, Resonators and Filters..

Micomachined antennas. Design, Fabrication and Measurements. Integration and Packaging for RF MEMS. Roles and types of Packages, Flip Chip Techniques, Multichip module packaging and Wafer bonding, Reliability issues and Thermal issues.

References :

1. RF MEMS – V K Varadan, A Laktakia and K J Vinoy, John Wiley, 2003 Reprint
2. RF MEMS Circuit Design J De Los Santos, Artech House, 2002
3. Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems, by Frank Ghenassia, Springer, 2005
1. Networks on Chips: Technology and Tools, by Luca Benini and Giovanni De Micheli , Morgan Kaufmann Publishers, 2006.