Thomas Karlo Blanco IV

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PORTFOLIO WEBSITE: https://arl7d.github.io/tkb4/

SKILLS / TOOLS / TESTERS / METHODOLOGIES:

- SQL, Python, R, C/C++, UNIX, TIBCO Spotfire, Tableau, MS Office, ETS364, ETS-88, VLCT, LTX Fusion/EX, Teradyne IFLEX, Lean Six Sigma (5S, DMAIC, KAIZEN), CAPA, 8D, 3x5Why, Statistical Process Control

EXPERIENCE:

Texas Instruments Philippines, Inc. — **Baguio, Philippines**

Test Engineering Manager (MGTS*) — **Feb 2018 – Jan 2020**

- Manage 3 separate teams: Tester Engineering (12 Engineers, 13 Techs), Test Systems Software (3 Engineers), Data Solutions Services (4 Software Developers). Facilitate annual employee performance reviews & provide guidance when needed.
- Align the team on daily priorities, initiate execution to meet schedules on projects, coordinate optimization efforts for continuous improvement on both hardware and software responsibilities, & drive for innovation.
- Coordinate with suppliers on both technical & commercial aspects of tester equipment which includes problem resolutions, upgrades, contract / service updates, continuous improvement initiatives, etc.
- Identify opportunities to increase productivity or to reduce cost by streamlining processes and systems.
- Lead the conversion/migration efforts of mature devices from legacy to roadmap test systems.
- Report weekly updates to senior management regarding key team performance metrics and projects.

Test Product Engineer – Test Start-up Lead Engineer (MGTS*) — **Feb 2015 – Feb 2018**

- Coordinate with both local (new products, assembly, quality) & external teams (from Dallas & China) on offloading SOT packaged devices into TI Philippines. Lead cross-functional teams to ensure smooth execution of key actions.
- Perform test characterization to qualify new hardware (Eagle Test Platform, Test interface), test programs, materials (fab, assembly) for production use. Worked with test developers to address yield concerns due to test program issues.
- Qualified TIPI's 1st ever SPC enabled system with both test & post-test log points in a single tester-turret-handler combo.
- Provide training to equipment techs on setup debug & production specialists lot loading procedures.

Test Product Engineer – Device Management — **Jan 2012 – Feb 2015**

- Managed various semiconductor products in terms of test yield stability, lot outlier analysis/dispositions, new test program release/offloads, checkout & debug, customer return analysis, material qualification, etc.
- Utilized several data mining & visualization tools like Spreadsheets, SQL & Spotfire to gain insights from test data with the aim of either improving yield, optimizing test setup performance, minimizing outlier lots, streamlining test processes, etc.
- Debug test setup / interface issues. Isolating if test failures are tester, material or interface related.
- Mentor interns & new hires. Provide training about basic test methods, data tools, test processes & methodologies.

PROJECTS:

- **Solving Hidden Hot Switching Issues at Test** – a special case of hot-switching where unit testing causes capacitors to be charged, providing a potential difference, thus causing premature breakdown of certain loadboard relays. This was solved by rerouting test lines via existing solid-state relays. Improved FPY by ~15%, project won TI technical symposium champion & PH best in test.
- **SOT Package Test Interface Design Improvements** – innovation was aimed to avoid device misalignment due to package debris build-up on interface contactor nest. Impact: ~10% FPY improvement, project accepted as TI Internal Patent (MIA)
- **Tester Engineering Team Skill Flexibility Plan** – implemented a buddy-buddy system for sharing test platform knowledge which has widened the team's skill set and has strengthened 24/7 support on all tester platforms across TI.
- **Point-based Project prioritization system** – due to the Data Solutions team's heavy load, this system had been implemented which would now consider aspects like: impact, urgency, complexity, etc., then prioritizes the projects based on its total score.
- **Save Rejects System** – an upgrade to the old reject saving process. Key features: timebound and durations are dictated by the system, saving rules can now be implemented & approval requirements on certain cases. Impact: productivity & space.
- **Addressing Low FPY due to Transient Signals from Parasitic Capacitance** – caused by a device pin set to float, which has been affected by loadboard parasitic capacitance, causing the device to reset randomly and produce transients on the output. Addressed by connecting said pin to supply, which sets fixed delay times. Improved FPY by ~25%, won 2nd place in symposium.
- **Fab related Continuity Outlier lot process improvement** – updated the test program to have a separate continuity test for pins that are known to have a fabrication related continuity defect. This has optimized outlier processing and reduced cycle time.

EDUCATION / CERTIFICATION:

- **Saint Louis University, School of Engineering & Architecture** — **Baguio, Philippines**
  - Bachelor of Science in Electronics & Communications Engineering (***Cum Laude***) — Mar 2011
- **Google Professional Data Analytics Certificate (Credential ID: HJBRQN5D4X52) - Coursera.org** — Mar 2022
- **Licensed Electronics Engineer | ECE Board Exam Passer (License No: 0048452) - PRC, Manila, Phils.** — Nov 2011

* MGTS (Member Group Technical Staff) – a designation for members of the TI Technical Ladder, which is a group of top technical employees within Texas Instruments.