

Computer Architecture (CS2323)

Semester-I, 2023-2024 (Aug - Nov 2023)

Administrivia and logistics

- Course credits: 3
- Teaching segments: 3-6 (7th Sep till 28th Nov)
- Instructor: Rajesh Kedia (rkedia@cse.iith.ac.in)
- TAs:
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- Lecture schedule: 3 hours a week, P slot (Mon 2.30-3.55 pm, Thu 4.00-5.25 pm)
- Lecture venue: A-LH2 (A-block, Ground floor)
- Instructor contact hours: Just after the lectures or by appointment
- Lab schedule: 2 hours per week in B524 (in two separate batches of 65 each). **TBD**
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- We will use [moodle](#) for course management (assignment, marks upload, quiz, etc.)
 - Login through IITH email account and enroll yourself in the course
- Academic honesty during the course is essential
- You are expected to read the textbook in addition to the lectures. Only selected lecture slides, which are not available in the book, will be made available.
- We encourage class participation in the form of classroom interaction as well as discussion over forum in moodle.

Pre-requisites

- Introduction to programming (ID1063/ID1303)
- Digital systems (concept of multiplexers, decoders, registers, etc.)
- Introduction to Data Structures (CS1353)

Course topics: Theory

While the topics would be introduced in general, we will use RISC-V to understand the specifics of an instruction set and the processor design. The following is a high-level outline of the topics.

1. Introduction
2. Instruction set architecture (ISA)
3. Processor design
4. Caches and memory hierarchy
5. Computer arithmetic
6. I/O interfacing
7. Recent trends and wrapup

Course topics: Lab and practical

The lab exercises would be primarily based on assembly language programming on RISC-V simulators and C-code to implement certain concepts being taught. We would have some lab related tutorials and hands-on sessions in the B524 lab. Some indicative assignments include:

1. Understanding various instructions
2. Assembly code development for common mathematical functions
3. Understanding various cache architectures and implementing related concepts
4. Interfacing with I/O devices

Lab Exercises in this offering:

1. Assembly: Basic assembly programming - addition/subtraction and familiarity with RIPES
2. Assembly: Decode the opcode and Identify the RISC-V Instruction type (R/I/B/S/J/U)
3. C/C++: RISC-V Disassembler - Convert a given RISC-V machine code to assembly code
4. Assembly, on board: Blinking LED on the Sparkfun RED-V board
5. C/C++: Pipeline stall detector
6. C/C++: Cache miss simulation
7. Lab exam: (a) GCD computation using assembly language
(b) Floating point addition using integer arithmetic

Evaluation components

1. In-class quizzes
2. Homeworks
3. Exam-1
4. Exam-2
5. Lab assignments
6. Lab quiz or Lab exam
7. Class participation

Late submission policy:

1. **HW:** Late submission upto 24 hours - 10% deduction. NO marks will be given for late submission beyond 24 hours.
2. **Quiz:** In-class and hence no late submission allowed.
3. **Labs:**
 - a. 10% deduction for delay of every 24 hours or part. Except for medical reasons, submission after a week of the designated lab slot will not be evaluated.

References:

1. Computer Organization and Design, The Hardware/Software Interface (RISC-V edition) by David A. Patterson and John L. Hennessy
2. The RISC-V Instruction Set Manual, Volume I: Unprivileged ISA, Document Version 20191213

3. Digital Design and Computer Architecture (RISC-V edition), By David Harris and Sarah Harris
4. Basic Computer Architecture (also available as Computer organization and architecture), version 2.1, By Smruti Ranjan Sarangi

Course schedule

https://docs.google.com/spreadsheets/d/14po8qARA63KEHij2j1YyP4oMsj2Tbdbe235V_znpFg_u

Updates

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