



It is forbidden to change the name of the variables or their order.

Question One (13 marks)

A) Choose the correct answer (10 marks)

1) 11011 – 101 using 1's complement equals.....

a) 10101	b) 10110	c) 00010	d) 11101
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2) If $F(A, B, C) = (A B' + C)'$, then $F'(A, B, C) = \dots\dots\dots$

a) $((A'+B).C')'$	b) $((A+B').C)'$	c) $(A'+B).C'$	d) $((A'+B)+C)$
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3) $F(X, Y, Z) = (XY+Z)' + Y'Z$, if DeMorgan's law is applied to the first complemented term, then the whole expression will be

a) $(X' + Y').(Z' + Y'Z)$
b) $(X+Y).Z' + Y'Z$
c) $((X'+Y') . Z').(Y+Z')$
d) $((X'+Y').Z') + Y'Z$

4) For a 4Mx16 RAM, the number of address lines will be equal to.....

a) 12	b) 16	c) 22	d) 4
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5) For a 4Mx16 RAM, the size of the internal decoder is

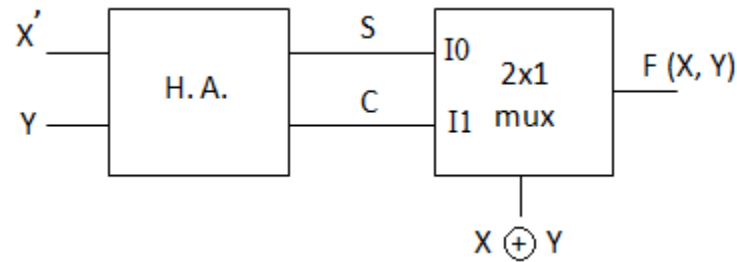
a) 12×2^{12}	b) 16×2^{16}	c) 22×2^{22}	d) 4×2^4
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6) For a 4Mx16 RAM, the number of input or output lines equals to

a) 4M	b) 16	c) 22	d) 8
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7) To construct 8Mx32 RAM, we need 4Mx16 RAMs

a) 2	b) 8	c) 12	d) 4
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8) According to the above circuit, the output S (X, Y) =.....

a) $\sum(0, 3)$	b) $\sum(1, 2)$	c) $\sum(1, 3)$	d) $\sum(0, 2)$
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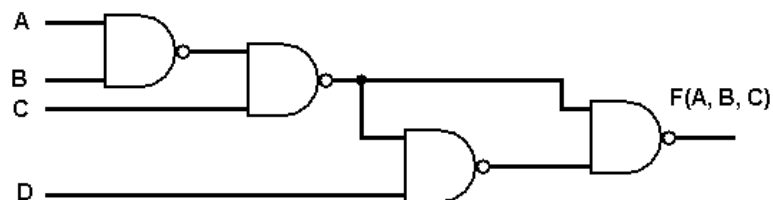
9) According to the above circuit, the output C (X, Y) =.....

a) $\sum(0, 3)$	b) $\sum(3)$	c) $\sum(1)$	d) $\sum(1, 2)$
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10) According to the above circuit, the F (X, Y) =.....

a) $\sum(1, 2, 3)$	b) $\sum(0, 1, 3)$	c) 0	d) $\sum(0, 3)$
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B) Convert the following NAND circuit to AND \ OR circuit (3 marks)



Question Two (14 marks)

A) Choose the correct answer (10 marks)

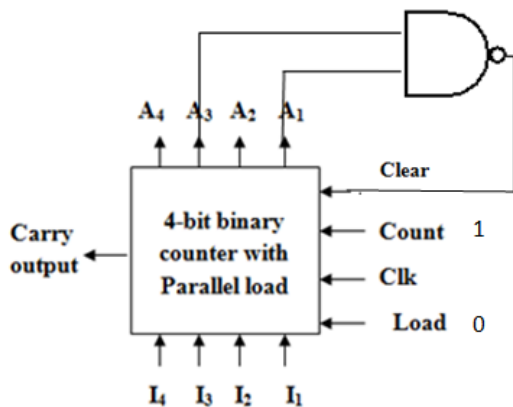
- 1) If the function $F(A, B, C) = \sum(0, 4, 6, 7)$ is implemented using 4x1 mux with A and C on selections then the inputs from I_0 to I_3 will be equal to respectively.

a) $B', 0, B', 1$	b) $0, 1, 0, 1$	c) $B', 0, 1, B$	d) B', B, B', B
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- 2) The simplest form for the Function $F(A, B, C, D) = (A+B') \cdot (A+C'+D)$ in sum of product equals.....

a) $A' B + A' C D'$
b) $A + B' D + B' C'$
c) $A + B' D + B' C' D'$
d) $A + A' B' D + A' B' C'$

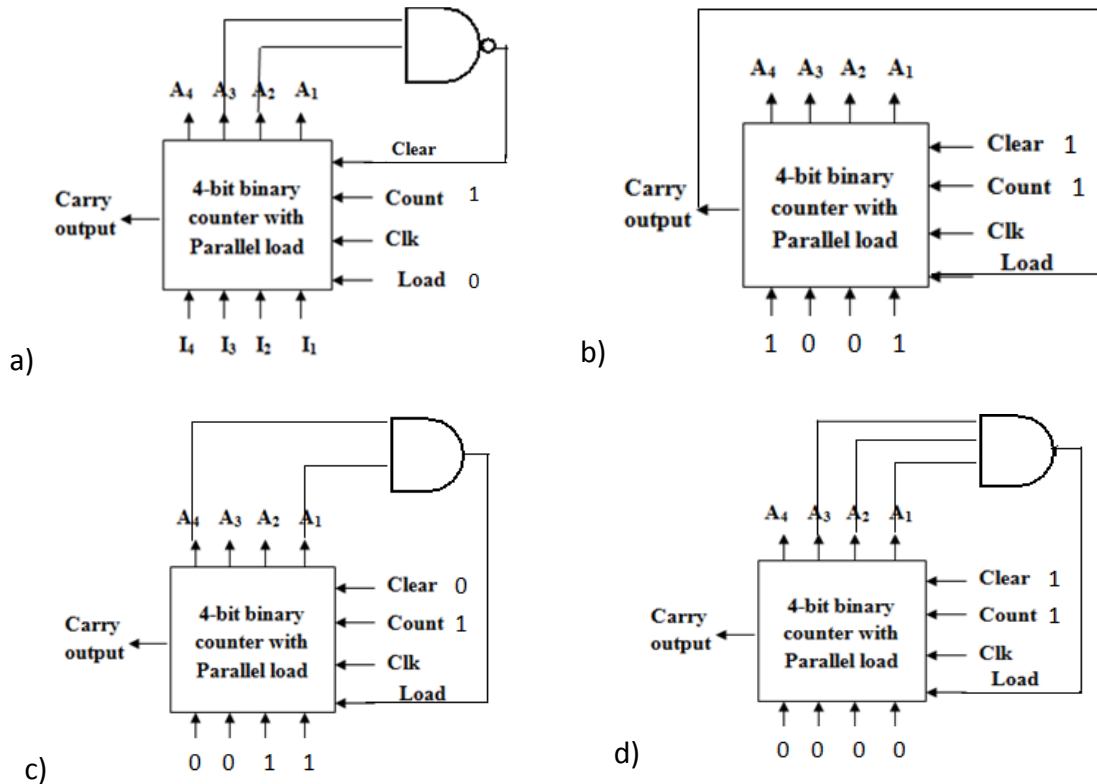
- 3) Using the following 4 bit programmable counter with the given function table, It will count



Clear	Clk	Load	Count	Function
0	X	X	X	Clear all
1	X	0	0	No change
1	↑	1	X	Load input count
1	↑	0	1	

a) From 0 to 15	b) From 0 to 10	c) From 0 to 5	d) From 0 to 4
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- 4) Using a 4 bit programmable counter with the same function table provided in the previous question, which case can give f/7?



5) Given a **lowest** priority 4x2 encoder, in order to have a value 1 0 on its outputs, its inputs D0 – D3 can be equal to respectively.

a) x, x, 1, 0	b) 0, 1, x, x	c) x, 1, 0, 0	d) 0, 0, 1, x
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B) Construct a 4 bit parallel load \ no change Register with the following function table using D flipflops and any needed external gates (4 marks).

Select	Function
0	Parallel load
1	No change

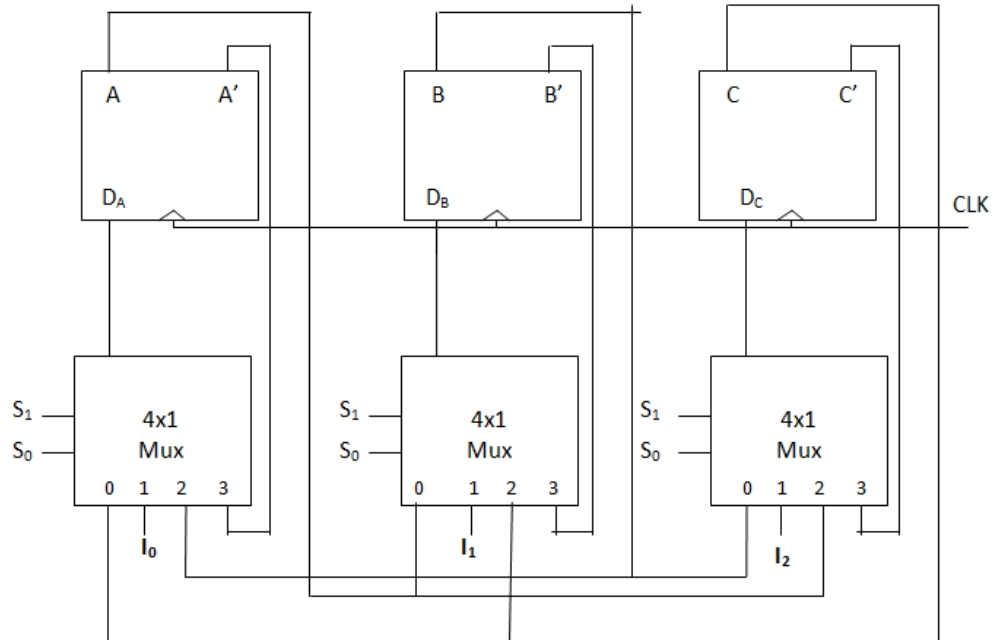
Question Three (15 marks)

- A) For the following Decimal-Code converter table from decimal code $X_3 X_2 X_1 X_0$ to decimal code $Y_3 Y_2 Y_1 Y_0$, find the Min-terms of the outputs and don't cares if exist. (6 marks)

Decimal	X_3	X_2	X_1	X_0
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	0	1
5	1	1	1	0
6	0	0	1	1
7	1	0	1	1
8	0	1	1	1
9	1	1	1	1

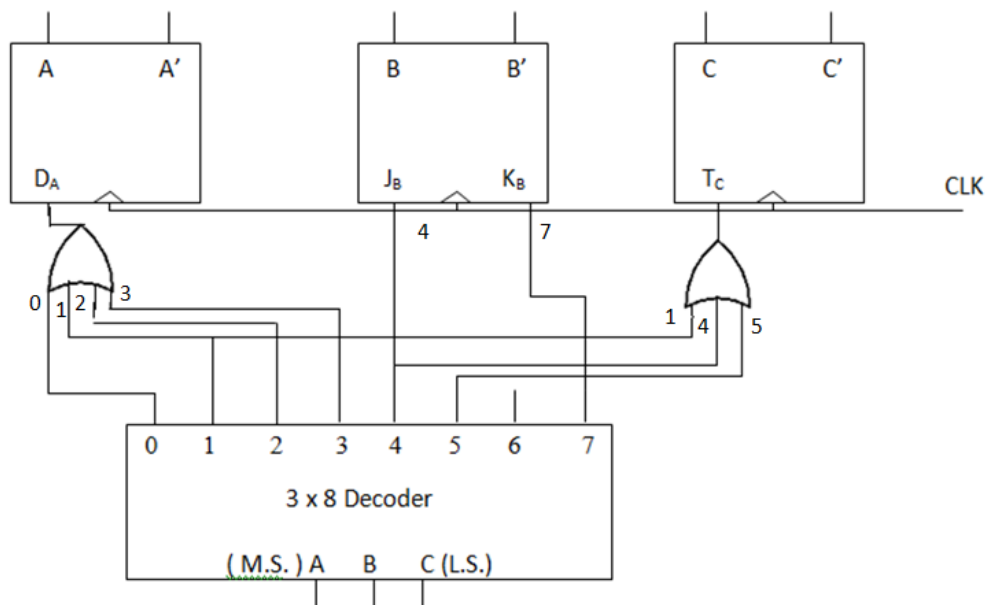
Decimal	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1

- B) Construct a 8x1 multiplexer using 4x1 multiplexers and one 2x1 multiplexer. (4 marks)
- C) Follow the circuit connections, then find the function table of the given universal shift register of 4-different functions. (All muxs have the same selection control). (5 marks)



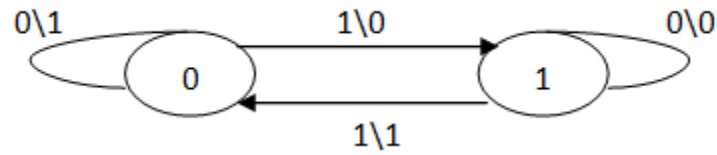
Question Four (18 marks)

- A) Design a counter that counts the following sequence 1, 6, 7, 3, 2 using T flipflops.
(8 marks)
- B) Analyze the following sequential circuit then find state table, state diagram and finally find the repeated sequence. Is it a self correcting counter (state your reasons)?
(10 marks)

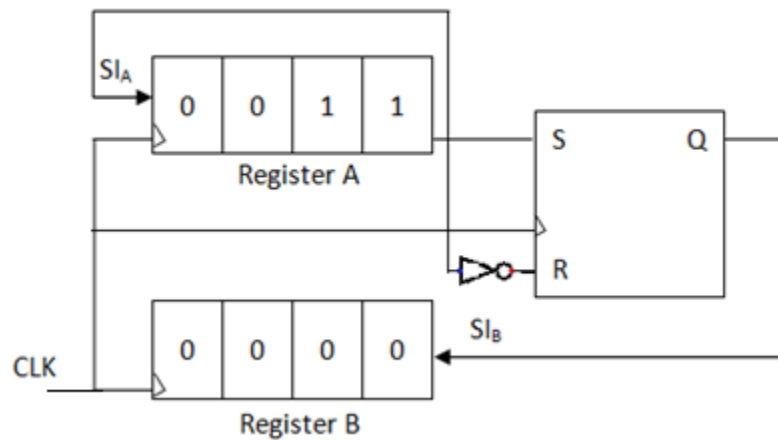


Question Five (15 marks)

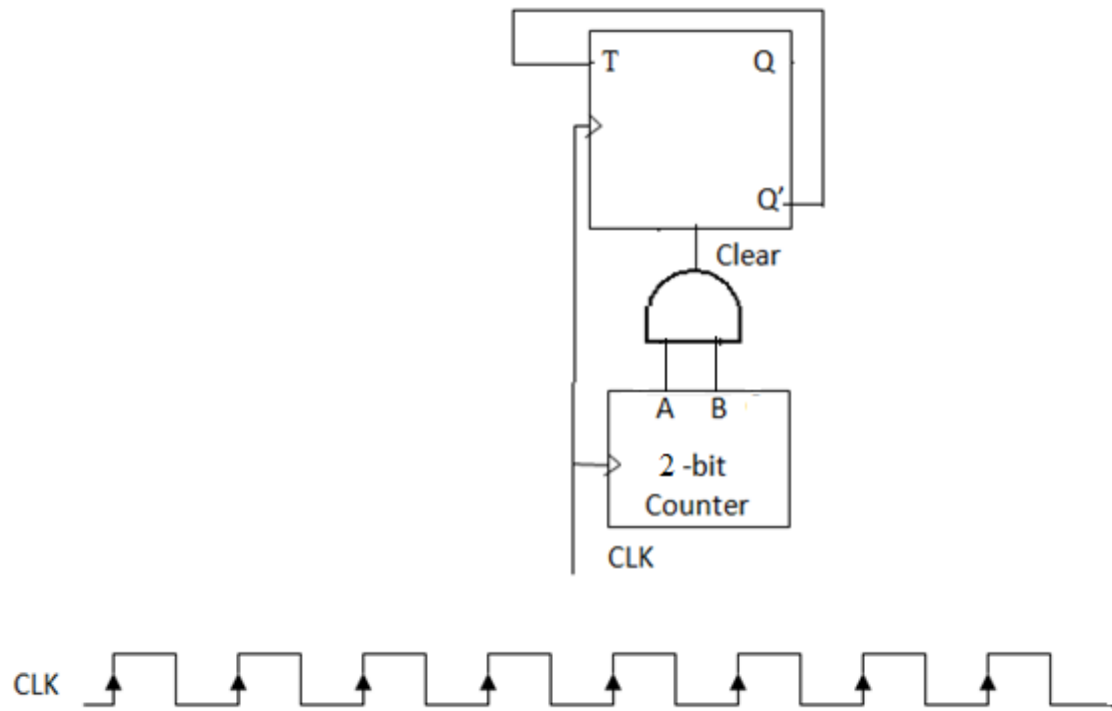
- A) Design a sequential circuit using JK flipflop according to the following state diagram. (5 marks)



- B) Find the content for the two 4 bit shift registers of the following sequential circuit during 4 clocks. [the initial value for Q is zero] (5 marks)



- C) Draw the output waveform Q for the given clock signal CLK. If the frequency of the CLK is 500 HZ what will be the frequency of the output Q? [the initial value for Q is zero] (5marks)



Good Luck ☺

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