Laying Out Standard Cells with Magic VLSI

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1. Setting the Grid

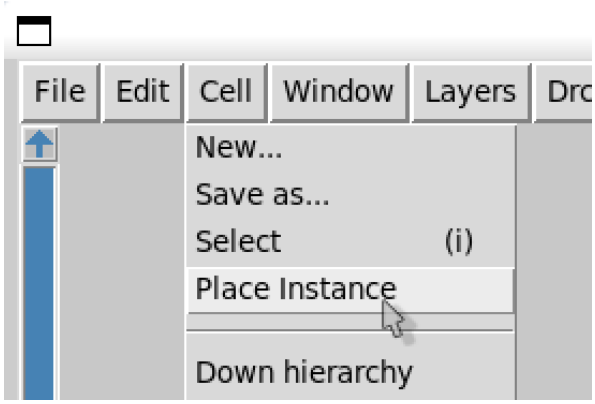
First, set set the grid to 0.46um by 0.36um and enable grid snapping by running the following commands:

```
grid 0.46um 0.34um
snap user
```

This grid size matches the "hd" (high density) cells - for other cell types, you can find the grid sizes in the **second** table in this page. The relevant rows are labeled "X-GRID" and "Y-GRID".

2. Instantiating the cells

To create an instance of a standard cell, select the "Cell" menu on top, and then "Place Instance":

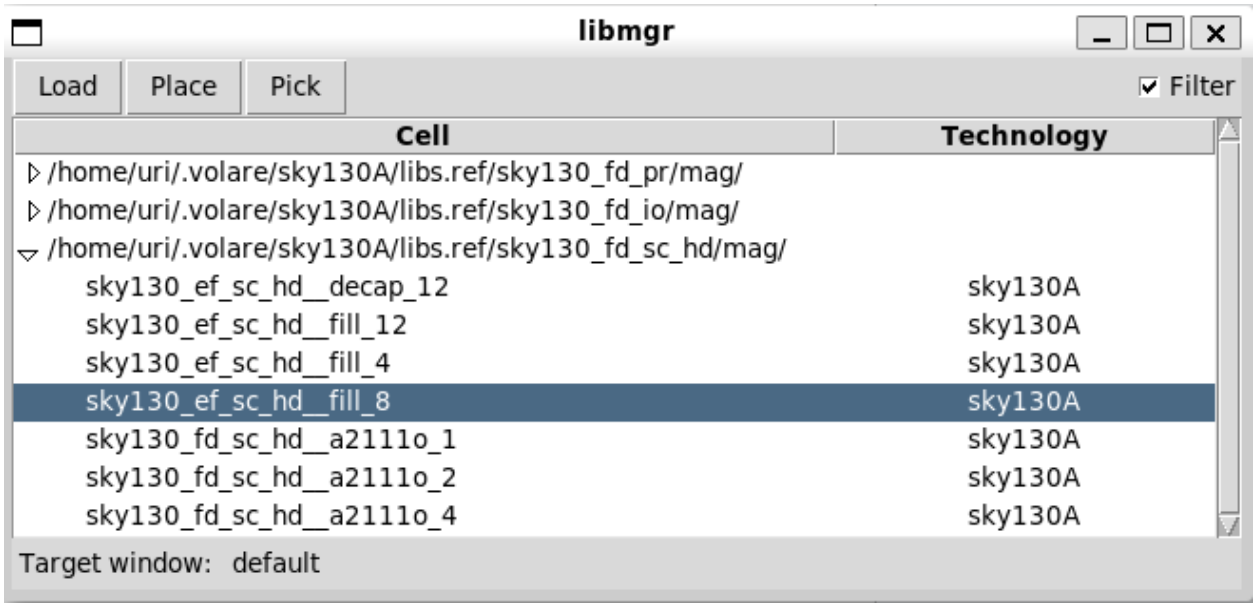


In the dialog that appears, type `$PDK_ROOT` to go to the PDK directory on your computer. Then type: `sky130A/libs.ref/sky130_fd_sc_hd/mag`

This will get you into the directory with all the standard cells.

You can select any cell you want to instantiate. If you want to filter the list, you can also type a word surrounded by asterisk signs. For instance, if you only wanted cells containing "xor" in their name, type `*xor*`.

As an alternative, you can browse the standard cell catalog in the "ligmgr" panel. Open the "Options" menu and select "Library Manager". You'll see a list of all the libraries and the cell inside. Select a cell and click "Place" to add it to your design:



If you know the name of the cell you'd like to place, you can also use the "getcell" command to place it, e.g.:

```
getcell sky130_fd_sc_hd__inv_1
```

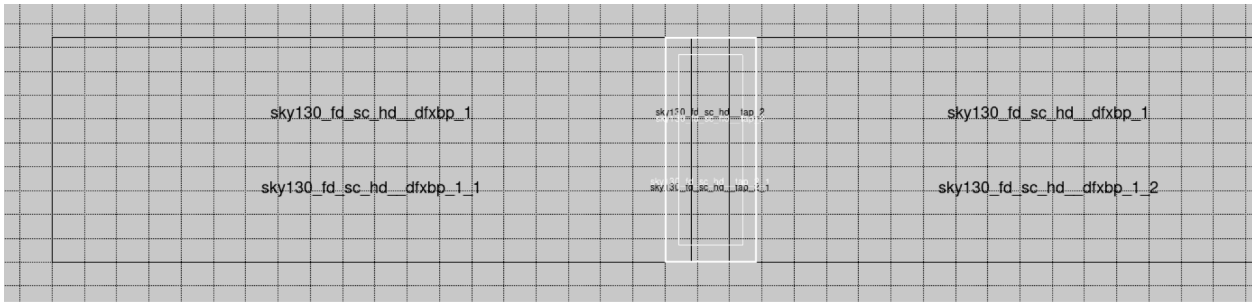
* The meaning of "sky130_fd_sc_hd" is as follows: sky130 - node name, fd - foundry, sc - standard cells, hd - high density.

3. Placing the cells

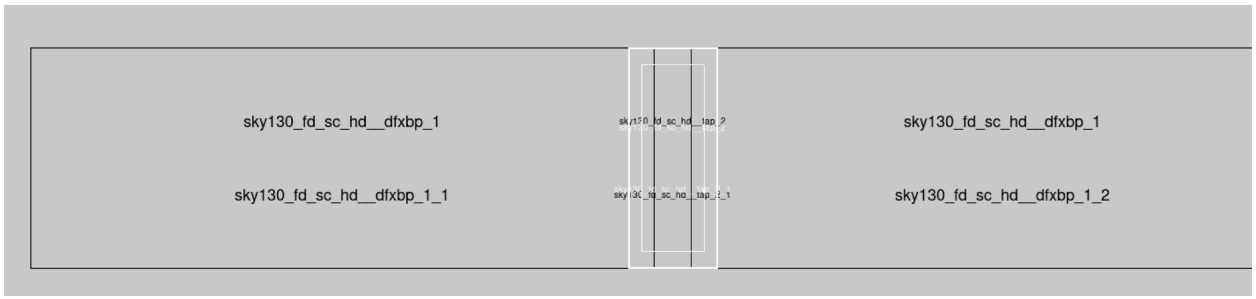
The standard cells are placed in rows. You must include a tap cell within 15um of every transistor (e.g. sky130_fd_sc_hd__tapvpwrvgnd_1), and the cells should slightly overlap each other. If you are missing tap cells, you'll get DRC errors.

Adhering to the grid settings defined above ensures the overlapping parts of the cells match - otherwise, you'll get DRC errors.

Here's an example of three cells placed, showing how they overlap. The outer white rectangle is a sky130_fd_sc_hd__tap_1, which partially overlaps the two surrounding cells.



Another screenshot, this time without the grid:

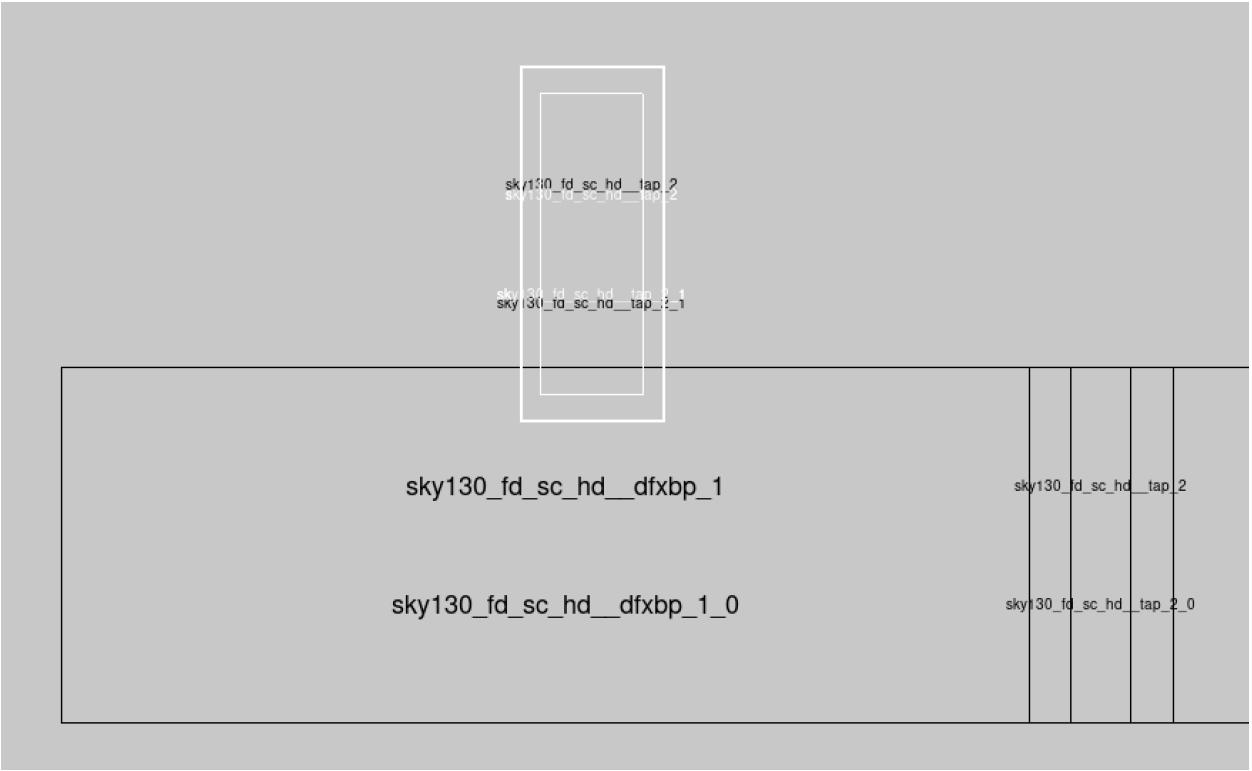


In this example, we're using the dfxbp cell, which is a delay flip-flop with complementary outputs.

Note: to show the contents of a cell, move the mouse over it, press i, and then press x (expand). To hide the contents of a cell (as in the screenshots above), press shift+x.

4. Placing multiple rows

You can stack multiple rows on top of one another by mirroring the cells vertically on every other row. To mirror a cell vertically, select the instance (by moving the mouse over it and pressing i), then press shift+f.
The cells should overlap each other, as shown in the screenshot below:



If you are getting DRC errors, you either forgot to flip the cells, or not snapping the cells to the grid as explained above.

5. Wiring the cells

Connect the **VPB** strip (on metal1) to power, and the **VNB** strip to ground. Then wire the various pins according to your schematic. In case of multiple rows, you will have to wire multiple strips.

For long strips, it's best to have several connection points, due to the resistance of the metal1 strip (~0.125Ω per square).