Advance Computer Architecture
(CS501)
Assignment # 01
Spring 2022

Total marks = 20
Deadline
16th of June, 2022

Please carefully read the following instructions before attempting the assignment.

RULES FOR MARKING

It should be clear that your assignment would not get any credit if:

- The assignment is submitted after the due date.
- The submitted assignment does not open or the file is corrupt.
- Strict action will be taken if the submitted solution is copied from any other student or the internet.

You should consult the recommended books to clarify your concepts as handouts are not sufficient.
You are supposed to submit your assignment in Doc or Docx format.
Any other formats like scan images, PDF, ZIP, RAR, PPT, BMP, etc. will not be accepted.

Topic Covered:

- The objective of this assignment is to increase the learning capabilities of the students about
  - Performance Measurement of a processor
  - Performance Comparison of processors
  - Classification of Instruction Set Architecture for different machines

NOTE

No assignment will be accepted *after the due date via email in any case* (whether it is the case of load shedding or internet malfunctioning etc.). Hence refrain from uploading assignments in the last hour of the deadline. It is recommended to upload the solution file at least two days before its closing date.

If you people find any mistake or confusion in the assignment (Question statement), please consult with your instructor before the deadline. After the deadline, no queries will be entertained in this regard.

For any query, feel free to email at:
cs501@vu.edu.pk

Questions No 01 — 10 marks

Write the instructions for 2-address machine and 3-address machine to evaluate the following expression.

$$Z = 2(X + Y) - 4XY$$

Note: x, y and z represent memory locations.

Solution:

2-address instructions:

```
load z, x
add z, y
mpy z, 2
load t, x
mpy t, y
mpy t, 4
sub z, t
```

3-address instructions:

```
add z, x, y
mpy z, z, 2
mpy t, x, y
mpy t, t, 4
sub z, z, t
```

Questions No 02 — 10 marks

Consider the following Assembly code written for SRC machine where t, a and b are memory locations and their value are t = 5, a = 4 and b = 38.

```
ld R1, t
addi R3, R1, 40
addi R3, R3, 2
shl R1, R3, 2
sub R2, R1, R3
ld R4, a
shl R5, R4, 4
sub R5, R4, R3
```

Registers	Contents
R1	
R2	
R3	
R4	
R5	

Solution:

Registers	Contents
R1	188
R2	141
R3	47
R4	4
R5	-43