SiEPICfab ZEP Platform

ThickZEP (ZEP 520A : 550 nm thick)

ThinZEP (ZEP 520A -7 : 250 nm thick)

(Template: SiEPICfab Shuksan PDK)

Overview

This document gives the details of the Zep PDK, technology process, the layer information, MPW runs and design software installation and support.

Goals

1. To design, fabricate and test air clad photonic devices on the thick Zep platform
2. To design, fabricate and test on chip laser integrated air clad photonic devices

Process Specifications

Silicon Waveguide:

The fabrication begins with a SOI wafer with a 220 nm silicon layer, 3.5 µm of oxide, on a 725 µm silicon handle wafer. Electron beam lithography (Jeol 8100FS) with a positive tone resist is used to define the patterns. The exposed silicon is etched fully down to the oxide with a vertical etch process.

Bond Pads and Electrical Routing:

Bond pads and electrical routing is carried out by patterning through the lift off process. 5nm of Titanium followed by 100nm of gold are deposited using Ebeam evaporation.

Shallow Trench for Laser Integration:

The final step in the photonic chip fabrication is to pattern and etch the shallow trench to create wells for laser die placement. The top silicon layer, BOX layer, and 75 microns of the silicon handle layer are etched away to create a shallow trench. 10 nm of titanium, followed by 100 nm of gold, are deposited and selectively removed using a lift-off process so that the metal remains only at the bottom of the trench and does not contact exposed silicon at any point during the processing.

Laser die attach:

The laser is attached using a flip-chip die bonder (Tresky T-3000 Pro), and indium for reflow soldering. This enables placement of the laser with an alignment accuracy within 5 µm.

Photonic wire bonding:

The photonic wire bond is written from the laser to the surface taper using Vanguard Automation's SONATA 1000. First a negative tone resist is dropcast on the chip, and the photonic wire bond is written using a pulsed-fs 780 nm laser. This enables a small volume of the resist to be polymerized via two-photon absorption, where this volume is rastered in

order to ‘print’ the freeform polymer waveguide. The un-exposed resist is then washed away using mild solvents, leaving only the photonic wire bond remaining.

Split-Passives

This run consists of the 220 nm thickness of silicon patterning with air cladded structures on SOI.

Split-Passives and Metal

This run consists of the 220 nm thickness of silicon patterning with air cladded structures on SOI with 5nm/100nm of Ti/Au metal layer on silicon as heaters.

Split-Lasers

This run consists of laser integration with the on chip silicon waveguide layer using photonic wire bonding.

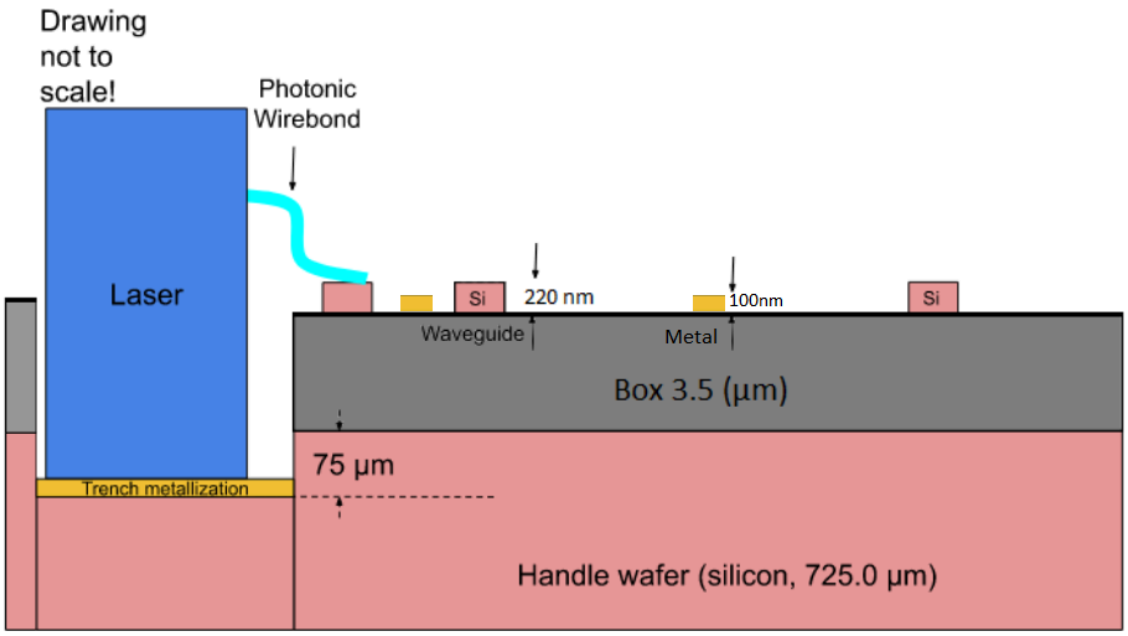

Figure 1:

Timelines (2023)

The following is the tentative timeline of the 2023 tape-outs with expected shipping date:

Date	Details, process splits in bullets	Expected completion
2023-01-16 SiEPICfab 23-01	• ThickZEP passives • ThickZEP passives + metal	• 2 week • 3 weeks
2023-02-21 SiEPICfab 23-02	• ThickZEP passives • ThickZEP passives + lasers	• 2 week • 6 weeks
2023-04-20 SiEPICfab Zep01	• Thin ZEP passives • Thin ZEP passives + metal	• 2 week • 3 weeks
2023-07-31 SiEPICfab Zep02	• Thin ZEP passives • Thin ZEP passives + metal • Thin ZEP passives + metal+metalized trench	• 4 weeks
2023-11-25 SiEPICfab Zep03	• Thin ZEP passives • Thin ZEP passives + metal	• 2 week • 3 weeks

Layer table

The following table provides a brief description of each of the available layers in the PDK.

Layer name	Layer/datatype	Description
Si_core	1/0	Layer to draw silicon waveguides; will be XORed with Si_clad.
Si_clad	1/2	Layer to draw the extent of the Si etch, including cladding and core.
Si_etch_highres	100/0	High Resolution Layer to draw fully etched trenches, but use SLS/Shape PEC. (trench)
Si_etch_lowres	101/0	Low Resolution Layer to draw fully etched trenches but use no-SLS or PEC. (trench)
M1	11/0	Layer to draw metal routing, heaters, etc
DeepTrench	201/0	Layer to define deep trench etch regions. For edge couplers
Floorplan	99/0	Marks the layout design area.
text	10/0	Text labels for automated measurements.
DevRec	68/0	Device recognition layer for DRC.

PinRec	1/10	Port/pins recognition layer for snapping and connectivity checks.
Waveguide	1/99	Virtual layer, guiding shape for waveguide, used for length calculation
SEM	200/0	Requests for SEM images. Rectangles in a 4:3 aspect.
EBL-Regions	8100/0	EBL Litho Manual Write Field Regions

Design Rules

Layer	**Minimum feature size**	**Overlay Accuracy**
Si	100 nm (thickZEP) 50nm (thinZEP)	N/A
Metal	5 µm	3µm

Table 2: Minimum Spacing between layers (exclusion, distance A and B must be separated by)

	Layer B	
Layer A	**Si**	**Metal**
Si	70 nm	4µm
Metal	-	5µm

Table 3: Overlap (area A and B must overlap)

	Layer B	
Layer A	**Si**	**Metal**
Si	-	-
Metal	-	-

Critical Dimensions Through SEM Images

Study of critical dimensions has been carried out using silicon island based (Figure 1a) and hole based (Figure 1b) structures, which are basically inverted designs of each other more clearly depicted through the SEM images in Figure 2. Both silicon box like shape and lines have been drawn for a width range between 40nm to 300nm with 50% density or 0.5 fill factor as shown in Figure 3. To study reproducibility, four copies of this design group have

been made in different location of the chip. After fabrication, SEM images have been taken of all the structures and measured through the open source software, ImageJ.

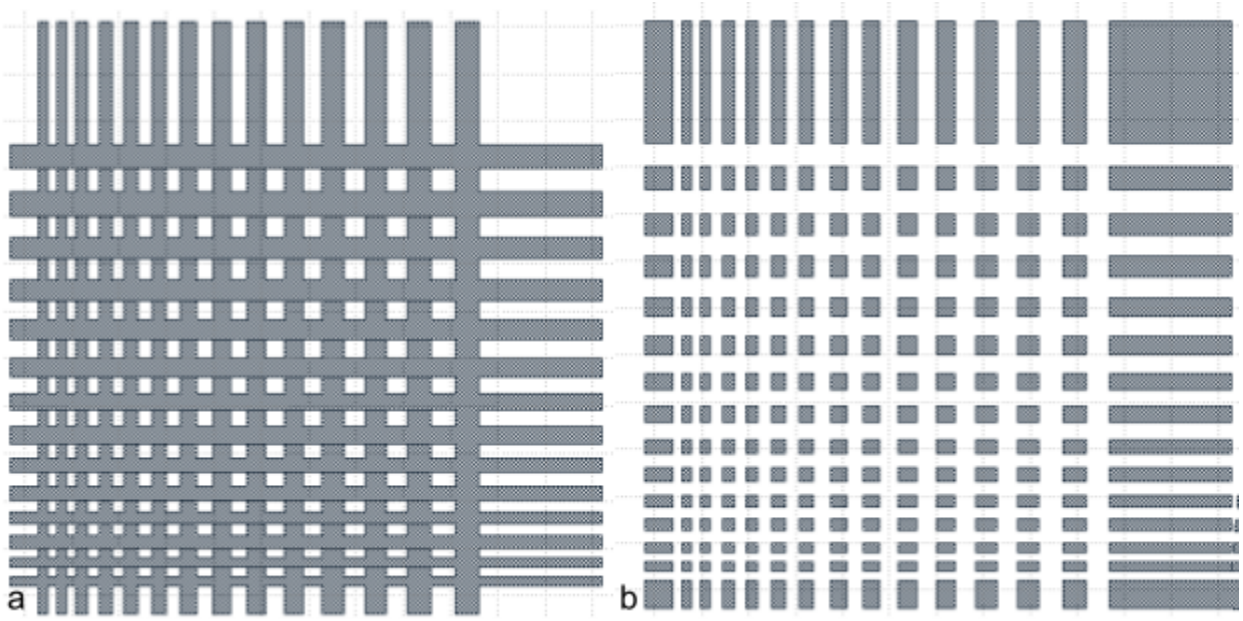

Figure 2: Design in GDS of a) island like structures and b) hole-based structures. The darker regions are the area of exposure which means for a positive resist as ZEP, these areas will have the resist removed after development and will undergo etching (remove silicon)

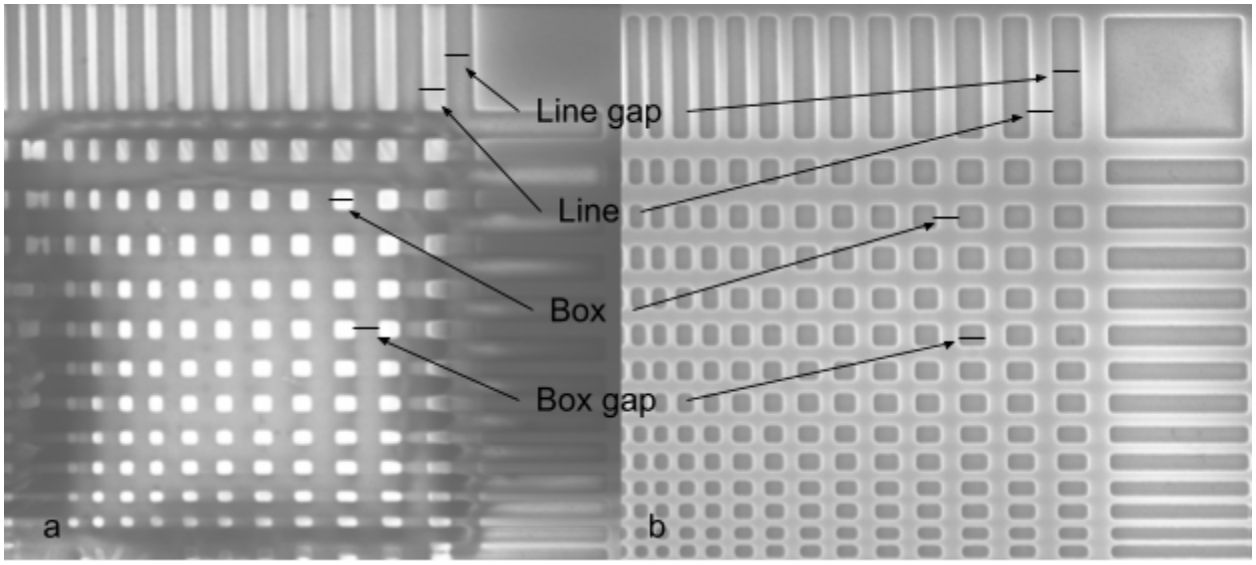

Figure 3: SEM image of the fabricated island (a) and hole (b) based critical dimension features representing drawn features between 120nm to 300nm. This image also defines the nomenclature for the graph in Figure 5.

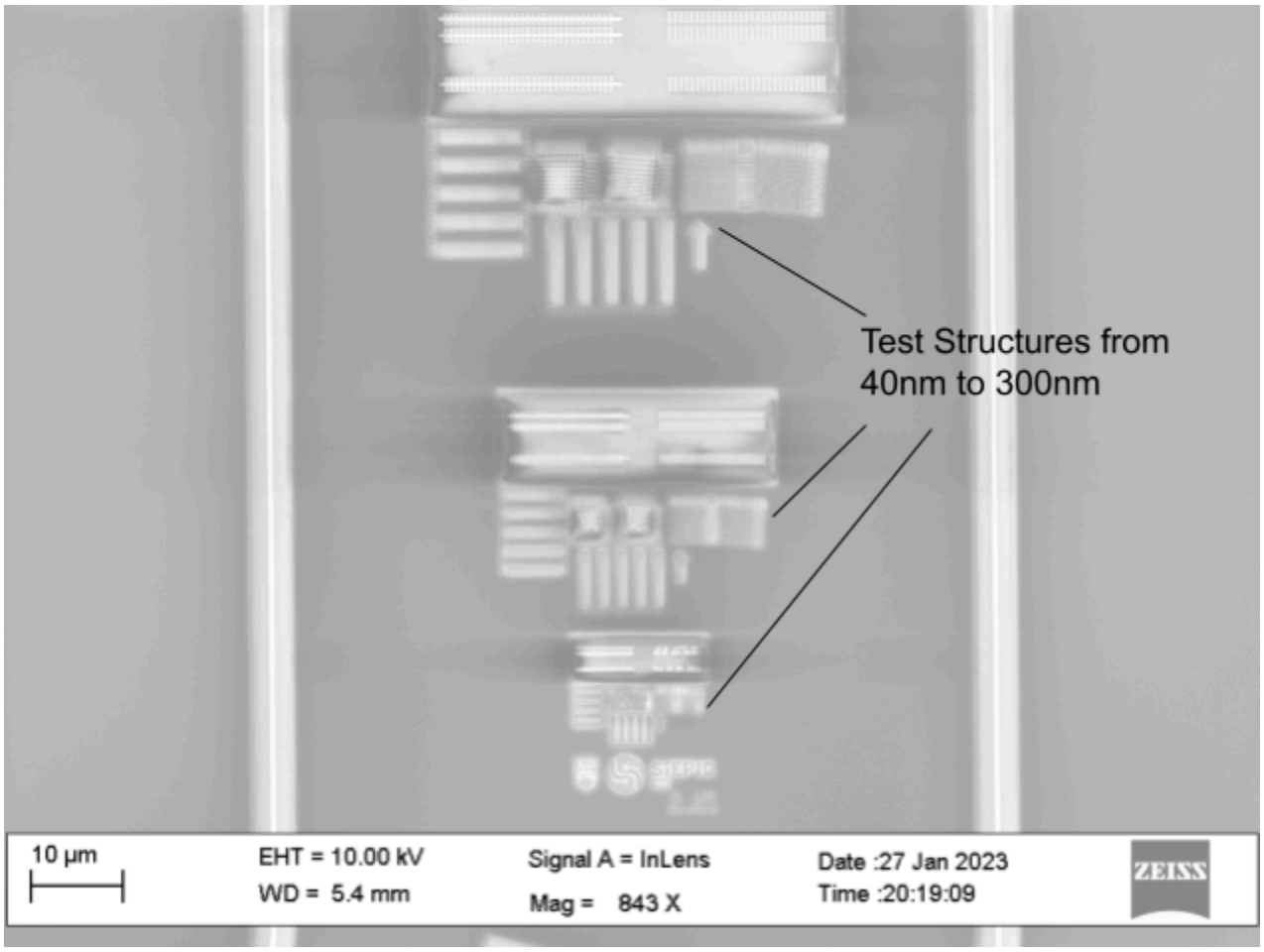

Figure 4: SEM Image of the test structures

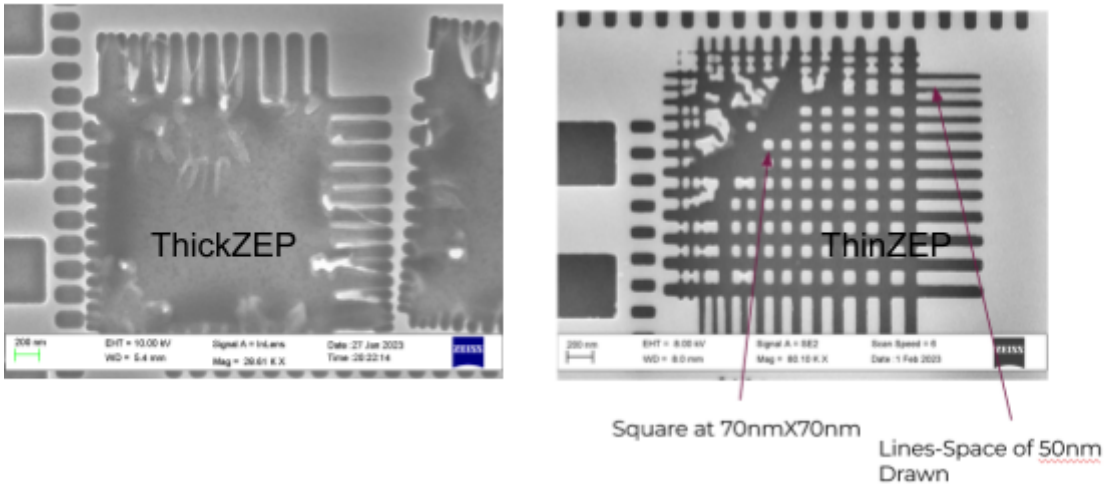

Fig: The thinZEP process provides a higher resolution by reproducing size 70 nm squares as minimum features and 50 nm line space resolved. The features failed in thickZEP process

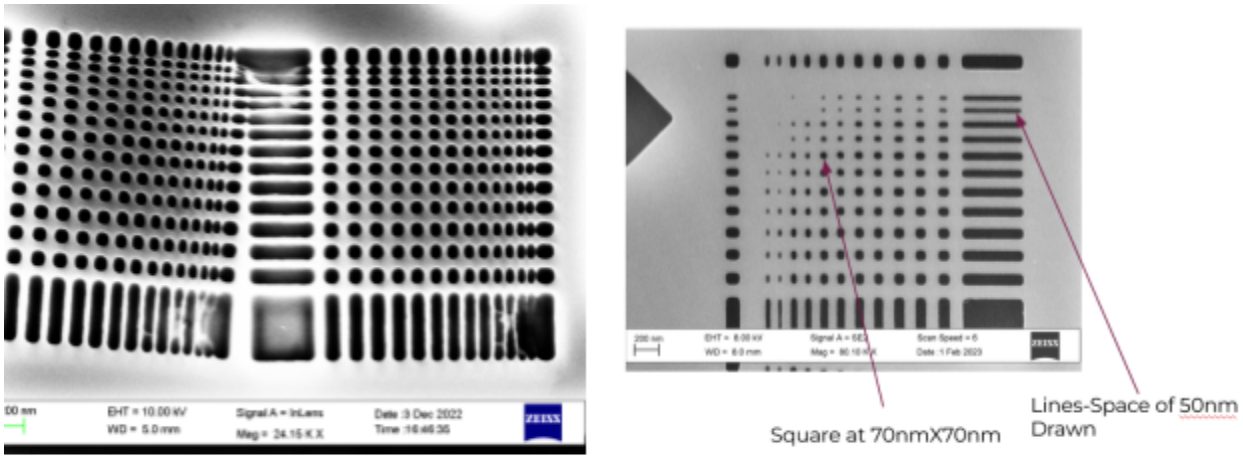

Fig: The hole based structures are resolved better in thickZEP process with even 40 nm squares resolved - the line spaces collapses however in this resolution. On the other hand, the line spaces works well till 50 nm. Square space (holes) lower than 60 nm are however not resolved in thinZEP due to a shrinking bias introduced in the Ebeam write data preparation

Process Bias through BRAGG gratings

Bragg gratings are two-port devices that operate as wavelength-selective reflectors. The below data show the results of a design-of-experiment in which several Bragg grating devices (designed with W=500 nm, ΔW=25 nm, number of gratings=500) with increasing Bragg periods. The results can provide an estimate of the process bias showing that designers should expect a 35 nm process bias (over-etching) for thickZEP while for thinZEP it is almost no bias.

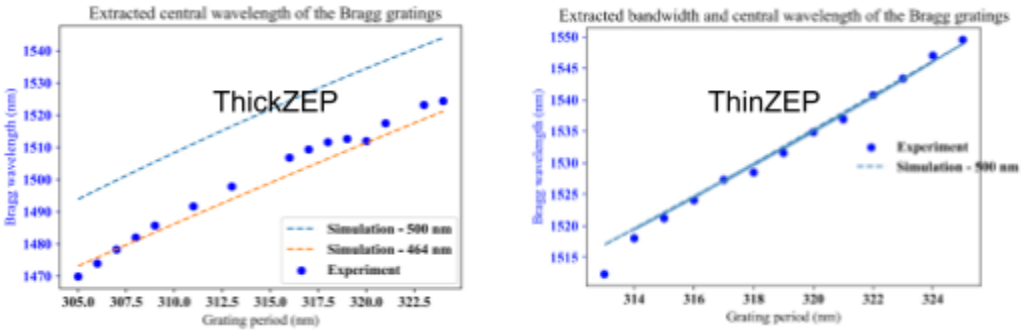

Fig: Process bias comparison between the two process shows about 35 nm over etching in thickzep and none in thinzep

Submission

- Design Rule check: please check using both:
  - KLayout SiEPIC > Verification > Design Rule Check (DRC) - SiEPICfab-ZEP

    - KLayout SiEPIC > Verification > Functional Layout Check
    - All the design rules should be considered as "warnings", and you do not need to obtain Waivers for violations
- File format: GDS or OASIS. Use the KLayout SiEPIC > Export for SiEPICfab-ZEP fabrication (flat)
    - this script performs the required layer boolean operations and basic clean-up

Automated Testing (Optional)

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Process Development Kit (PDK)

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Historical Process Control Parameters

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Split-Passive

Waveguides (straight and bent):

THICKZEP PROCESS						
Date			2022 10 02	2022 11 03	2022 11 26	2023 01 14
Type	Wavelength (nm)	Polarization	Loss (dB/cm)			
Straight	1550	TE	2.12 ± 0.18	3.56 ± 1.59	2.55 ± 0.16	None
Spiral	1550	TE	2.44 ± 0.21	4.81 ± 0.09	3.97 ± 0.32	6.18 ± 0.69

THINZEP PROCESS							
Date			2023 04 21	2023 04 20	2023 07 31	2023 11 25	
Type	Wavelength (nm)	Polarization	Loss (dB/cm)				
Straight	1550	TE	1.44 ± 0.17	2.68 ± 0.17	2.98 ± 0.19	2.65 ± 0.31	2.47 ± 0.3
Spiral	1550	TE	3.22 ± 0.71	3.48 ± 0.10	4.48 ± 0.17	5.11 ± 0.42	3.43 ± 0.07

Components:

- Grating couplers: Insertion loss, bandwidth
- Y-branches: Cutback
- Ring resonators
- Directional couplers with varying splitting ratios
- Broadband directional couplers
- Strip-to-slot converters
- Waveguide crossings
- Bragg gratings

Split-Lasers

Surface tapers coupling efficiency

Laser LIV curves

Development Roadmap

- Expand current C-band PDK
- Create O-band PDK
- Create compact models library for simulation
- Additional process options
    - Split-Actives with cladding and metallization
    - Split-Modulator with polymer modulators
- Automated Electro-optic lasers testing
- 200 mm wafer flow

Appendix

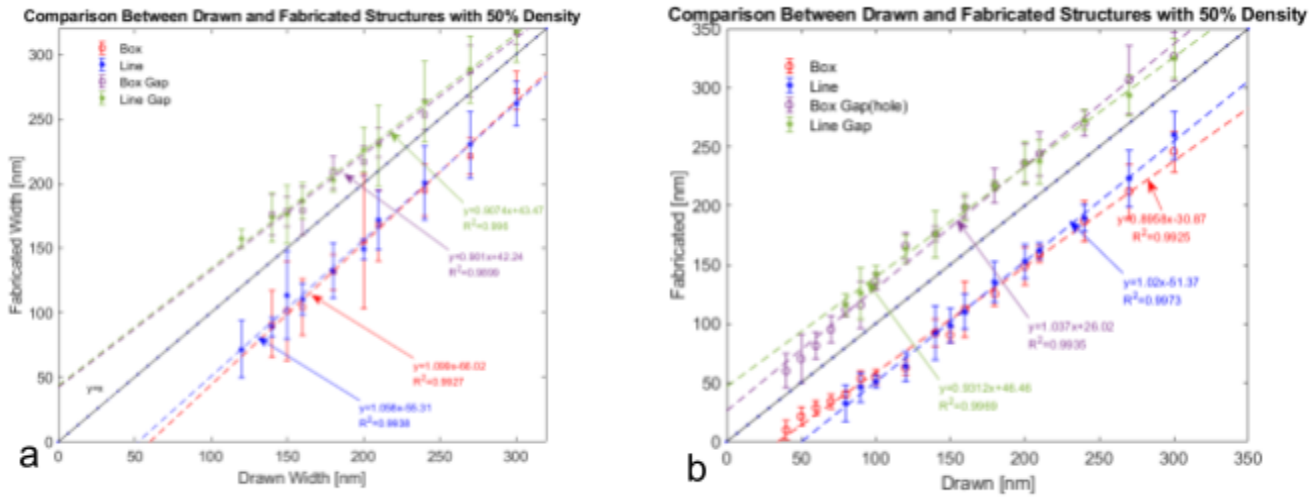

Figure A1: Fit data for the CDs for island like (a) and hole based (b) design for thickZEP

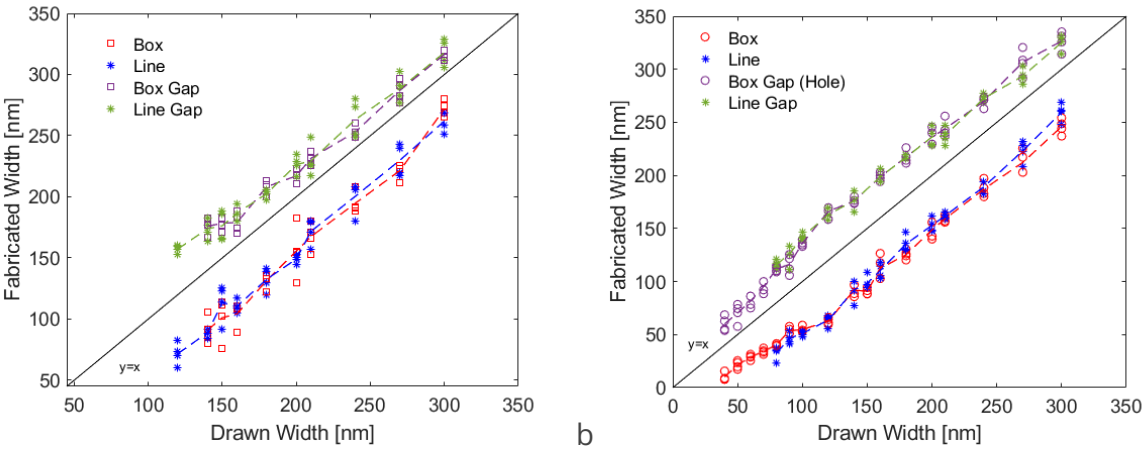

Figure A2: The graphs showing all the measured data points for each drawn critical dimension for the thickZEP process. The dotted lines show the average. An average bias (over etching) of 45±5nm is observed for drawn silicon regions. For the gaps, the bias is less and ranges between 20nm to 30nm approximately.

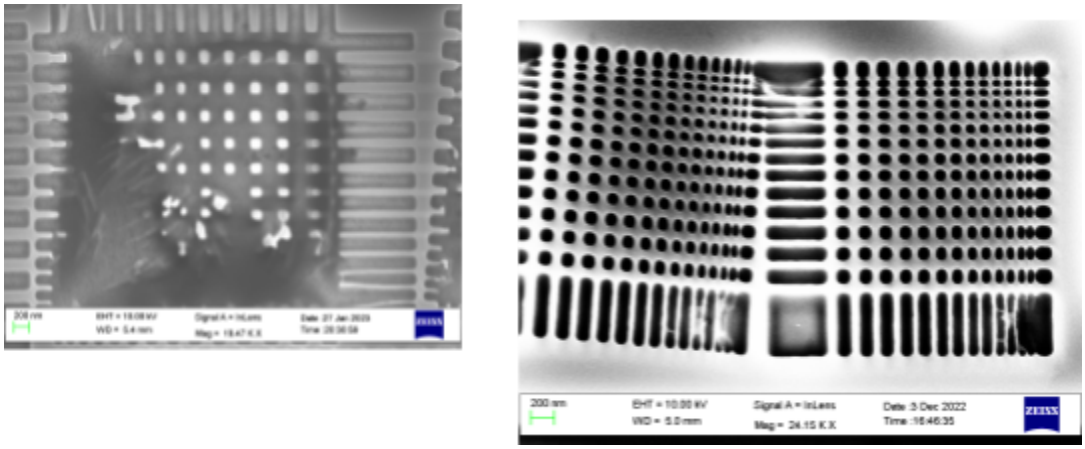

Figure A3: The images show how the critical dimensions fail to resolve in lower limits for thickZEP