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NEW SCHEME

11763

Reg. No.

Seventh Semester B.E. Degree Examination, January/February 2006

Instrumentation Technology

DSP Architecture

Time: 3 hrs.

Note: 1. Answer any FIVE full questions.
2. All questions carry equal marks.

1. (a) What are decimation and interpolation as used in DSP works ? Why are they used? Briefly explain each one of them with a block schematic for illustration. Let $x(n) = \{0, 3, 6, 9, 12\}$ be interpolated using $L = 3$. If the lowpass filter used has $h(n) = \{1/3, 2/3, 1, 2/3, 1/3\}$, find the interpolated sequence. (10 Marks)

(b) With neat sketches for illustration, discuss briefly the following building blocks that are essential to carry out DSP computations.

i) Barrel shifter ii) MAC unit. (10 Marks)

2. (a) What is the difference between a microcoded program control and a hard wired program control ? Why is the later preferred for DSP implementations ? (6 Marks)

(b) What is pipelining ? With neat illustrations comment on the implementation of an 8-tap FIR filter using -

i) one MAC unit,

ii) a pipelined structure. (10 Marks)

(c) Compute the sequence in which the input data should be ordered for a 16-point DIF FFT. (4 Marks)

3. (a) Which is the architecture used in $TMS320\ C54_{XX}$ processors ? How is the $TMS320$ family divided ? Indicate the major functional units of '$C54_{XX}$ device. List the addressing modes of '$C54_{XX}$ processors. (10 Marks)

(b) Illustrate the bus usage of '$C54_{XX}$ for read and write accesses in a table. (6 Marks)

(c) Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82 are 1, 2, & 3,

$$LD\ *AR3+,\ A$$
$$ADD\ \#1000h,\ A$$
$$STL\ A,\ *AR3-$$

(4 Marks)

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NEW SCHEME

Seventh Semester B.E. Degree Examination, Dec. 06 / Jan. 07
IT
DSP Architecture

Time: 3 hrs.] [Max. Marks:100

Note : Answer any FIVE full questions.

1 a. With block diagram, explain the scheme of a digital signal processing system. (08 Marks)

b. Fig.1(b) shows the front end of a simple data acquisition system. Determine the minimum sampling frequency F_s to give an aliasing error of less than 2% of the signal level in the passband.

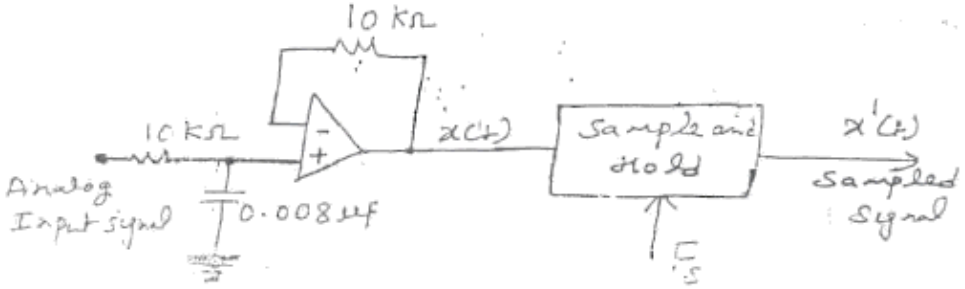

Fig.1(b) (06 Marks)

c. Explain the steps to be followed to convert the sampling rate by a non-integer factor. (06 Marks)

2 a. What is barrel shifter? Implement a 4 bit shift left barrel shifter. (10 Marks)

b. Indicate and explain the addressing mode provided in the architecture of DSP to implement real time signal processing algorithm. (10 Marks)

3 a. With block diagram, explain the working of a program sequence provided in the architecture of a DSP. (10 Marks)

b. With functional diagram, explain the central processing unit of the TMS 320C54XX processors. (10 Marks)

4 a. What is the configuration of on-chip DARAM onchip SARAM and ROM if

i) MP/$\overline{MC}$ = 0 , OVLY =1 and DROM = 0

ii) MP/$\overline{MC}$ = 1, OVLY = 1 and DROM = 1

for TMS 320C5416? (10 Marks)

b. Write a program to compute the sum of three product terms given by the equation $y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$;

Where h_0, h_1 and h_2 are constants and x(n), x(n-1) and x(n-2) are input samples. (10 Marks)

Contd.... 2

5 a. What is Q-notation? Compute the values represented by the 16 bit fixed point number N = 4000 h in the Q15 and Q7 notations. (08 Marks)

b. Develop the TMS 320 C54XX program to implement the following IIR filter :

$$H(Z) = \frac{(0.1+0.2Z^{-1}+0.1Z^{-2})(0.5-0.2Z^{-2})}{(1+0.25Z^{-1})(1-0.15Z^{-1}-0.5Z^{-2})}$$ (14 Marks)

6 a. What is Butterfly configuration in a DFT computation? Explain. Also determine the followings for a 128-point FFT computations :

i) Number of stages

ii) Number of butterflies in each stage

iii) Number of butterflies needed for the entire computation. (10 Marks)

b. Design a data memory system WCR address range 000800R – 000FFFH for a C5416 processor. Use 2K×8 SRAM memory chips. (10 Marks)

7 a. Write TMS 320C54XX code to show how the DMA channel 5 context registers can be initialized. Choose arbitrary values to be written to the registers. (08 Marks)

b. With necessary diagrams, explain general and transient operation in a synchronous serial interface between the C54XX and a CODEC device. (12 Marks)

8 a. With block diagram, explain the functioning of a multi channel buffered serial port (MCBSP). (10 Marks)

b. Give the overview of JPEG algorithm used in an image processing system. (10 Marks)

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4. (a) With a neat block diagram for illustration, explain the circular addressing mode for '$C54_{XX}$' processors. (10 Marks)

(b) Explain briefly the following instructions of '$C54_{XX}$' with an example.

i) $MAC[R]$ Smem, Src

ii) MPY Smem, # lK, dst

iii) $RPTZ$,

iv) $MACD$ Smem, pmad, Src

v) LD Smem, 16, dst. (10 Marks)

5. (a) Write a program to compute $y = mx + c$ using the instructions of '$C54_{XX}$' processor. (7 Marks)

(b) Describe in detail the implementation of an interpolation filter with '$C54_{XX}$'. (13 Marks)

6. (a) Discuss the requirements with regard to the implementation of a general DITFFT butterfly in-place computation structure. Why should the data be scaled down before or during a butterfly computation ? (6 Marks)

(b) Write a '$C54_{XX}$' routine that can be used to implement the butterfly computation. (9 Marks)

(c) Write a '$C54_{XX}$' code to transfer a block of data from the program memory to the data memory. Following are the specifications :

Source address	: 2000h in program space
Destination address	: 0700h in data space
Transfer size	: 1000h single (16-bit) words
Channel use	: DMA channel # 0

(5 Marks)

7. (a) What is the purpose served by the synchronous serial interface of the '$C54_{XX}$ DSP'? With a schematic for illustration, explain how such an interface can be used for an analog input/output CODEC device. (12 Marks)

(b) What is McBSP ? Comment about this on the TMS320 C5416 DSP. What is its use ? Briefly describe the McBSP of $C54XX$. (5 Marks)

8. (a) Why, there is an explosion of applications in which commercial programmable DSPs are becoming more and more powerful ? (4 Marks)

(b) Explain briefly the following :

i) ECG signal processing for heart rate determination

ii) JPEG decoder. (16 Marks)

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5 a. Explain the scheme for updating filter coefficients in the adaptive filter implementation. (06 Marks)

b. With a block diagram, algorithm and TMS320c54x code, explain the implementation of a PID controller. (08 Marks)

c. Explain the poly phase sub filter scheme used to implement an interpolating filter. (06 Marks)

6 a. Explain the memory space organization of TMS320c54x processor. (06 Marks)

b. Interface a 4K x 16 and a 8K x 16 SRAM memory bank to TMS320c5416 processor with starting addresses 010000 h and 020000 h respectively. (08 Marks)

c. Discuss the 3 types of parallel I/O operations available in TMS 320c5416 processor. (06 Marks)

7 a. Write an instruction sequence to initialize the serial port McBSP2 in the TMS320c5416 processor. (06 Marks)

b. With a block diagram explain the internal architecture of the codec interface circuit PCM3002. (06 Marks)

c. Using flowcharts/algorithms explain the use of McBSP – DSP interface for the simple application of signal loop back (that is read a signal applied to ADC and write back to DAC). (08 Marks)

8 a. With a block diagram explain the implementation of a DSP based biotelemetry receiver system. (07 Marks)

b. Describe the algorithm for pitch detection in speech. (07 Marks)

c. Explain the process of JPEG encoding (06 Marks)

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Seventh Semester B.E. Degree Examination, Dec.08/Jan.09
DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. A signal x(t) is sampled at 8kHz. If 500 samples of this signal are used to compute the Fourier transform x(k), determine the frequency spacing between adjacent x(k) elements and find the analog frequency (in Hz) corresponding to K = 60 and 202. (04 Marks)

b. Write a MATLAB program to design a third order butterworth lowpass filter (for a sampling frequency of 2000Hz and a cut-off frequency of 500Hz) and to plot the designed filter frequency response. (06 Marks)

c. With a neat figure explain the structure of a 4 x 4 Braun multiplier. (06 Marks)

d. Using block diagram show the implementation of a 8 x 8 multiplier using 4 x 4 multipliers as the building blocks. (04 Marks)

2 a. It is required top find the sum of 256 numbers, each represented by 16 bits. Find the size of the resulting sum. If six LSBs of the above sum are truncated, (to prevent overflow) what is the error in the computation of the sum? (04 Marks)

b. Explain the organization of the on-chip memory in a DSP processor. (06 Marks)

c. For the following instructions specify the type of addressing mode. Also in each case compute the memory address of the operands and the contents of the addrreg after the memory accets. The initial contents of the addrreg and offsetreg are 620h and 040h respectively. i) ADD + * addrreg; ii) ADD *addrreg, offsetreg; iii) ADD * addrreg. (05 Marks)

d. Explain the pointer updating algorithm used for the circular addressing mode. (05 Marks)

3 a. With a neat block diagram explain the functional architecture of TMS320c54xx processor. (08 Marks)

b. Explain with suitable examples the following data addressing modes of TMS320c54xx processor i) Accumulator addressing, ii) Memory mapped register addressing; iii) Direct addressing. (06 Marks)

c. Explain the operation of the following instructions i) MPY # 41h, A; ii) RPTZ A, # N; iii) DELAY * AR3; iv) STH A, 1, * AR3 (06 Marks)

4 a. Write a TMS320c54xx program to find the average of eight 16 bit consecutive numbers stored in data memory. (08 Marks)

b. Derive the scale factor of 2.414 used with the butterfly computation. (05 Marks)

c. Determine the number of complex additions multiplications required for computing N = 8 point DFT using direct and radix - 2 FFT algorithms. (03 Marks)

d. Explain the computation of the signal spectrum, given the N – point transform x(k). (04 Marks)

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IT763

Seventh Semester B.E. Degree Examination, Dec. 07 / Jan. 08
DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Explain a digital signal processing system with typical signals in a DSP scheme. (06 Marks)
b. The equation $y(n) = 0.5\,x(n) + 0.5\,x(n-1)$ describes a simple FIR filter whose out put is the average of the current input x(n) and the past input x(n-1). Write the block diagram and sketch the magnitude frequency response and phase frequency response. (06 Marks)
c. With block diagram explain the ALU of a typical DSP devise. (08 Marks)

2 a. Explain the different cases that arise in updating the pointer in circular buffer addressing mode. (08 Marks)
b. With neat diagram explain the system level parallelism and pipe lining using.
i) Single MAC implementation of an 8-tap FIR filter.
ii) Pipelined implementation of an 8-tap FIR filter using eight MAC units. (12 Marks)

3 a. With neat diagram explain the functional diagram of the central processing unit of the TMS 320 C54 xx processor. (10 Marks)
b. Explain the block diagram of the indirect addressing mode of TMS 320 C 54 xx processor using dual memory operands. (06 Marks)
c. Assuming the current content of AR_3 to be 200 h, what will be its contents after each of the following TMS 320 C 54 xx addressing modes is used? Assume that the contents of AR_0 are 20 h.
i) $*AR_3 + 0B$
ii) $*AR_3 - 0B$. (04 Marks)

4 a. Explain the six stage pipe line operation of TMS 320 C 54 xx execution. (10 Marks)
b. Explain the Q–notation to multiply two Q_{15} number. (06 Marks)
c. What values are represented by the 16 bit fixed point number N = 4000 h in the Q_{15} and the Q_7 notation. (04 Marks)

5 a. Explain the implementation of PID controller of basic DSP algorithm. (10 Marks)
b. With reference to overflow and scaling implement an 8 point FFT structure, scale factor for all buffer files = ¼. (10 Marks)

6 a. Design an interface to connect a 16 k × 16 flash memory to a TMS 320 C 54 xx device. The processor address bus is [illegible]. (10 Marks)
b. Explain with a flow chart of interrupt handling by the DSP processor. (10 Marks)

7 a. With neat block diagram explain McBSP of C 54 xx. (10 Marks)
b. Determine the timing parameters for a 16-bit data communication in a DSK configured for a clock divisor of 6. The oscillator clock (CODEC – CLK)is at 12.288 MHz. (10 Marks)

8 a. Explain the ECG signal processing for heart rate generated by the DSP telemetry receiver from PPM signal. (10 Marks)
b. Explain the block diagram of a clipping auto correlation pitch dector. (10 Marks)

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