# Comments for IF04 (TDAQ) Snowmass Summary Report

[https://snowmass21.org/_media/instrumentation/snowmassbook-if04_v2.0.pdf](https://snowmass21.org/_media/instrumentation/snowmassbook-if04_v2.0.pdf)

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# Comments/Notes on IF04 Snowmass Parallel Session

- Readout links:
  - field must study, develop rad tolerant links. Industry won't do
  - Maintain small in-house developments for some circuits to help drive industry (nice if US had something like at CERN)
- Innovations in TDAQ:
  - Need for integration test centers
  - Need for TDAQ/detector system simulation, particularly for event-driven readouts
- Tracking triggers
  - Essential place where TDAQ and detector design can be done together
  - Do we need to focus on learning languages better matched to FPGA development: HLS lowers the bar for development/testing ideas, but not the most optimized
  - Need for pixel tracking in trigger (and knock-on effects with pixel chip designs and bandwidth challenge). Pixel stub design?

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**Comments**: I don't think that you raised the issue that a lot of the next generation FPGA chips (such as Xilinx versal) are going away from the paradigm of all programmable logic, to partially programmable logic with AI engines. This hampers the latency of the algorithms, but improves the overall compute. As part of the recommendations, we should support a study of next generation processor technologis in the context of Trigger/DAQ and understand the latency limitations (and consequently future detector buffer size).