VLSI DESIGN

VLSI → Very large scale integration design.

→ Electronics is characterised by reliability, low power dissipation extremely low weight and volume & low cost & copes easily with high degree of sophistication & complexity.

→ The integrated circuits made possible the design of powerful & flexible processors, which provide intelligent & adaptable devices.

→ The invention of transistor by William B. shockley, walter H. Brattain & John Bardeen of Bell laboratories was followed by development of Ic.

The very first Ic emerged at beginning of 1960 and since that time, there have been 4 generations of Ic.

1) SSI (small scale integration) (10–100)
2) MSI (Medium scale integration) (100–1000)
3) LSI (Large scale integration) (1K–20K)
4) VLSI (Very large scale integration)

↳ Upcoming 5th generation ULSI (Ultra large scale integration) characterized by complexity in excess of 3 million devices on a single Ic chip.

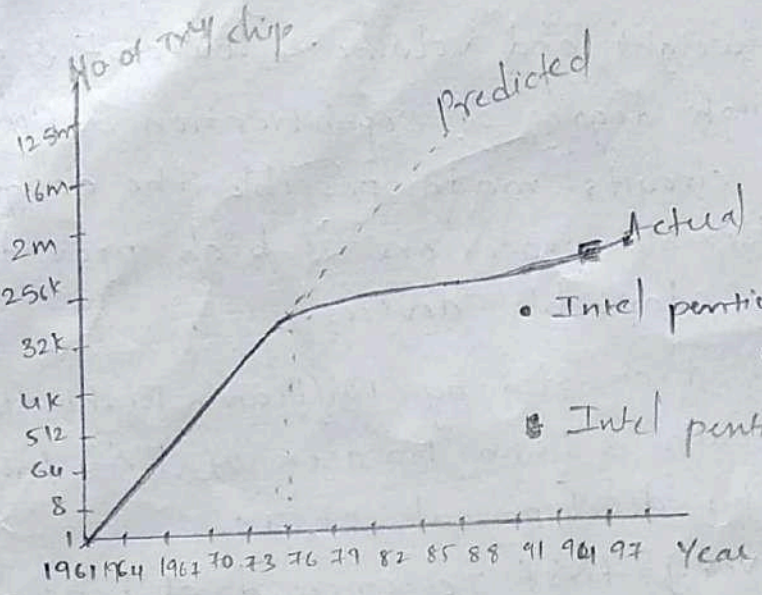
Ic Era:-

The potential of silicon Ic, has been an extremely rapid growth in the number of transistors being integrated into circuits on a single sibicon chip.

In less than 5 decades, this number has risen from tens to millions.

The relation between the number of trs per chip versus year, has become the "moore's 1st law".

The increase in no. of tx's double for every 2 years is known as "moore's 1st law" by Gordon moore in 1960's



* Over the past several years, silicon cmos technology has become the most dominant fabrication process for relativity high performance & cost effective VLSI circuits.
* The increase in no. of chips is highlighted by recent products such as RISC chips, in which it is possible to process 35 million instructions/sec.
* In particular emerging, Gallium Arsenide (GaAs) based technology will be most significant for ultra-high speed logic.

Microelectronics Evolution

Metal-oxide-Semiconductor (MOS) VLSI Technology

Within bounds of MOS technology, the possible circuit realizations may be based on

→ PMOS, NMOS, CMOS & BiCMOS devices

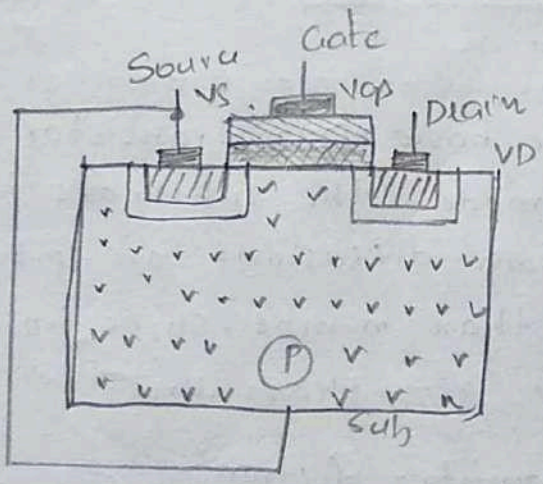
Basic MOS Transistors:-

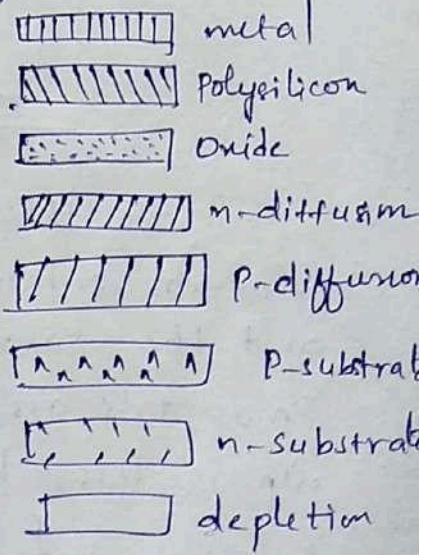
Nmos Enhancement & depletion mode transistors

→ Nmos devices are formed in a P-type substrate of moderate doping level. The source & drain regions are formed by diffusing n-type impurities through suitable masks into these areas to give desired n-impurity concentration & give rise to depletion regions.

→ Thus, source & drain are isolated from 1 another by 2 diodes. connects are made by deposited metal Layer.

Consider Enhancement mode first,





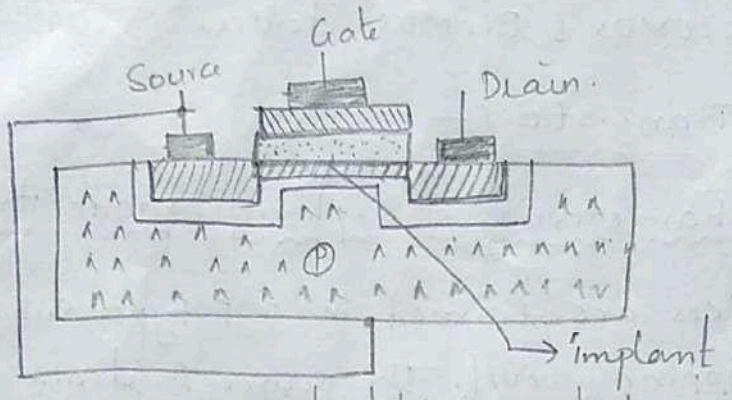
(a) nMOS Enhancement mode transistor.

The above figure shows a basic enhancement enhancement mode device in which the channel is not established & device is in non-conducting condition, $V_D = V_S = V_{GS} = 0$.

→ If the gate is connected to a stable positive voltage,

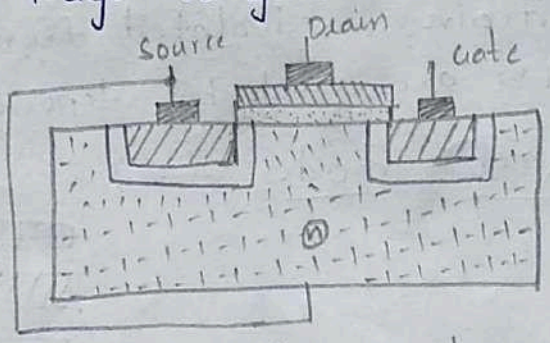
w.r. to source, then electric field established between gate (3) and substrate gives rise to charge inversion reg^n in substrate & conducting path / channel is formed b/w source & drain

→



n-mos depletion mode transistor.

Here, in depletion mode, the source & drain are connected by a conducting channel, under condition $V_{gs} = 0$, by implanting suitable impurities in region between source & drain. The channel can be closed by applying suitable negative voltage to gate.



Pmos enhancement mode transistor.

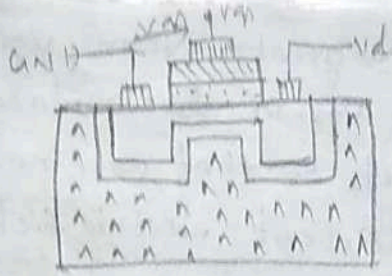
In this case, the basic PMOS transistor structure for an enhancement mode, the substrate is of n-type and the source & drain diffusions are p-type.

Pmos tx's are slower than n-mos, since hole mobility μ_p is less, by approx 2.5, than μ_n.

Enhancement mode transistor Action:-

To Understand the mechanism of Enhanced mode, we have to consider 3 conditions.

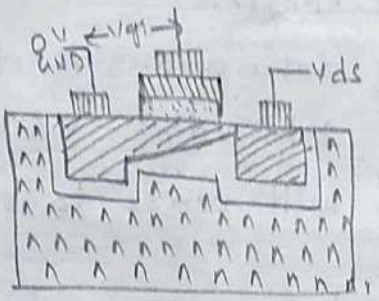
Threshold voltage (V_t):- The minimum voltage applied between gate & source to establish channel.



$V_{gs} > V_t$

$V_{ds} = 0V$

Fig. indicates the conditions prevailing with the channel established but no current flowing between source & drain. ($V_{ds} = 0$).



$V_{gs} > V_t$

$V_{ds} < V_{gs} - V_t$

Now, consider the conditions prevailing when current flows in the channel by applying a voltage V_{ds} between drain and source.

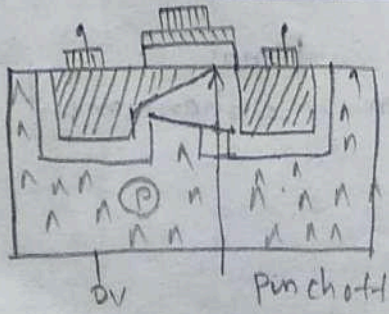
→ Along the channel, a corresponding IR drop = V_{ds}, will be there.

→ This results in the voltage between gate & channel varying with distance along the channel with the voltage being a maximum of V_{gs} at source end.

→ Since, the effective voltage is $V_g = V_{gs} - V_t$ (no I flows when $V_g < V_t$), there will be voltage ~~Vg~~ available to invert the channel at the drain end, so long as $V_{gs} - V_t \geq V_{ds}$.

→ The limiting condition comes when $\boxed{V_{ds} = V_{gs} - V_t}$.

if $V_{ds} < V_{gs} - V_t$, device is in non-Saturation region of operation is, $\boxed{V_{ds} < V_{gs} - V_t}$.



$V_{gs} > V_t$

$V_{ds} = V_{gs} - V_t$.

If V_{ds} is ↑d to a level greater than $V_{gs}-V_t$.

In this case, an IR drop = $V_{gs}-V_t$ takes place less than whole length of the channel, so that over part of channel near drain, there is insufficient electric field available to give rise to inversion layer to create channel, i.e Pinch-off.

→ Diffusion current completes the path from source to drain in this case, causing the channel to exhibit a high Rx & behave as a constant I-source.

→ This region is known as saturation, is characterized by almost constant, 'I' for ↑ in V_{ds}, $V_{ds} = V_{gs}-V_t$.

→ In all the cases, channel will cease to exit & no I will flow, $V_{gs} < V_t$.

→ Typical values, enhancement mode

$V_t = 1V$ for $V_{DD} = 5V$

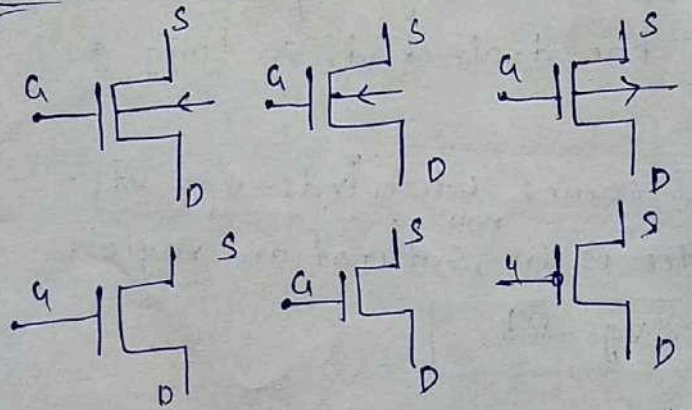
$V_t = 0.2 V_{DD}$.

Depletion mode Transistor Action:-

For depletion mode, devices channel is established because of implant, even when $V_{gs} = 0$ & to cause the channel to cease to exist a -ve voltage, V_{td} must be applied blw gate & source.

~~V_{td} << coescV_{DD}~~,

Symbols for nmos & Pmos Transistor.-



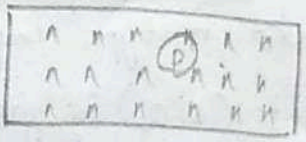
n-mos enhancement nmos depletion P-mos enhancement

N-Mos fabrication:-

→ Processing is carried out on a thin water cut from a single crystal of silicon of high purity into which required P-impurities are introduced as crystal is grown.

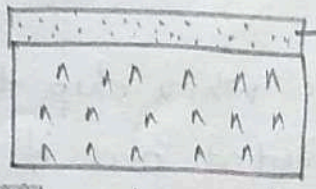
→ Such waters are typically 75 to 150mm in diameter and 0.4mm thick and are doped with, boron to impurity concentrations of $10^{15}/cm^3$ to $10^{16}/cm^3$.

1.

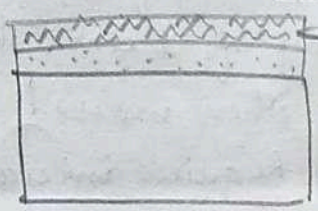


→ A sio_2 layer of 1 um thick grown on water surface acts as barrier to dopants while processing.

2.



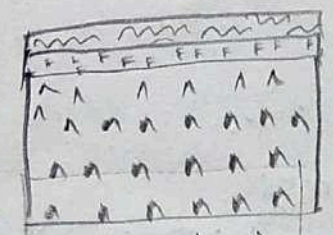
3.



→ The surface is now covered with photoresist deposited on wafer surface.

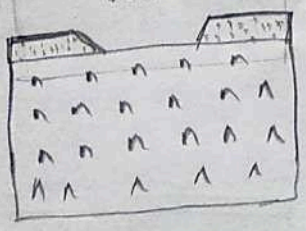
4.

→ photoresist layer is exposed to uv light through mask, which defines regions, where diffusion takes place.



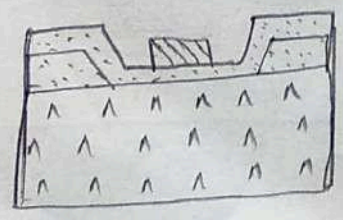
⇒ These areas are subsequently readily etched away together with underlying silicon dioxide, so that the wafer surface is exposed in window refined by mask.

5.



→ The remaining photoresist is removed & thin layer of si_2 (0.1um) is grown over entire chip & polysilicon is deposited on top, to form a gate structure

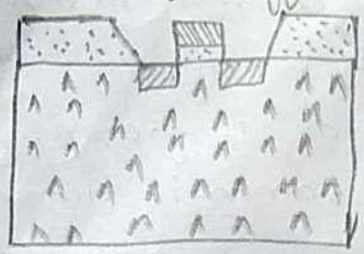
6.



→ Polysilicon layer consists of heavily doped

(7) polysilicon deposited by chemical vapour deposition (CVD)

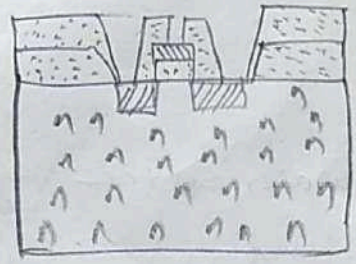
7. n+ diffusion



contact holes

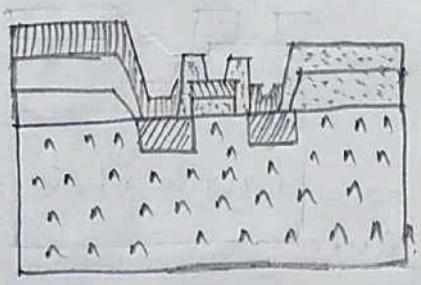
→ Photoresist coating & masking allows polysilicon to be patterned & then the thin oxide is removed to expose areas into which n-type impurities are to diffused to form source & drain. Diffusion is achieved by heating wafer to a high temperature & passing a gas containing the desired n-type impurity.

8.



→ Thick oxide (SiO_2) is grown all over again & is then masked with photoresist & etched to expose selected areas of polysilicon gate & drain & source areas.

9. pattern metallization



→ The whole chip then has metal deposited over its surface to a thickness typically of 1 um. This metal layer is then masked & etched to form required interconnection process.

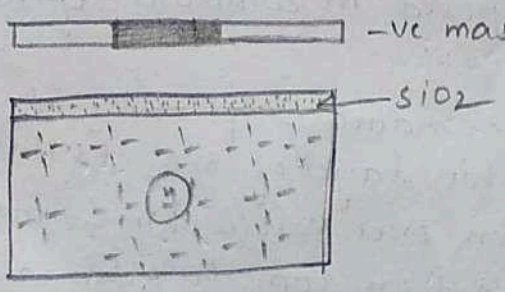
CMOS Fabrication:-

There are number of approaches to cmos fabrication.

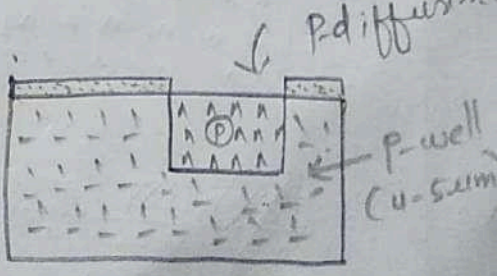
They are
1. P-well process.
2. n-well process
3. Twin tub process.
4. Silicon-on-insulator (SOI) process.

P-Well Process:-

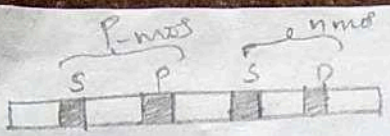
(1)

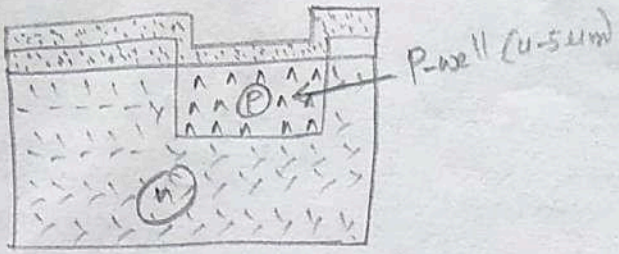


(2)



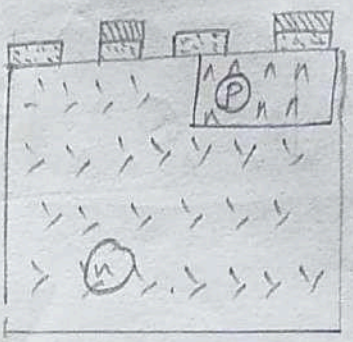
(3)



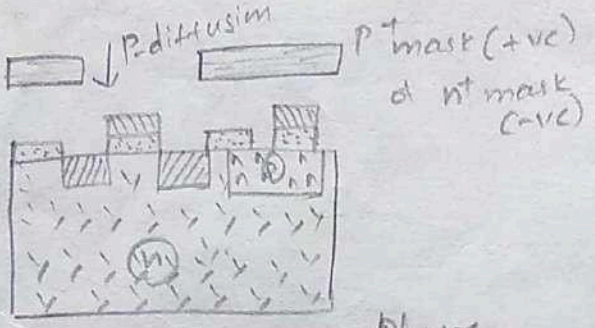


masks for source & drain
— for both nmos & pmos

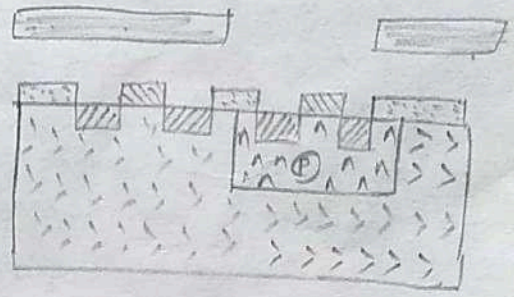
(4)



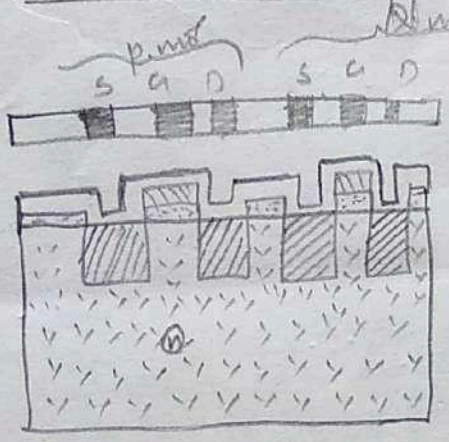
(5)



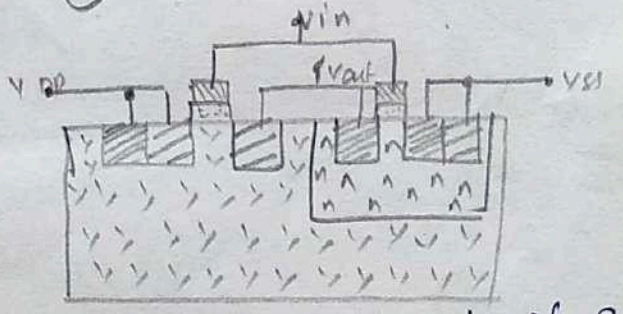
(6)



(7)



(8)



In P-well cmos fabrication, structure consists of an n-type substrate in which P-devices may be filmed by suitable masking & filming, diffusion.

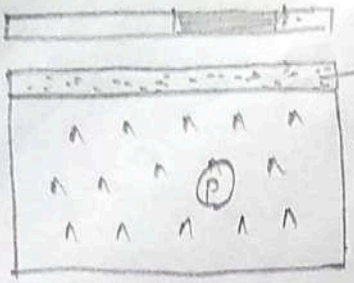
→ The diffusion may be carried out with special care since the P-well doping concentration & depth will affect the threshold voltages as well as breakdown voltages of n-transistors.

Cmos n-well Process

— these are superior to P-well b'cz of lower substrate bias effects on transistor threshold voltage (V_T) & lower parasitic Capacitances.

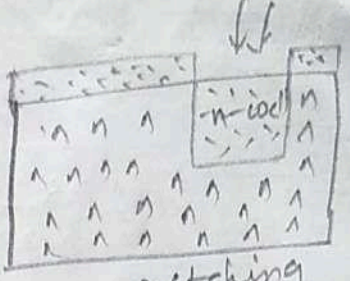
Fabrication steps :-

(1)



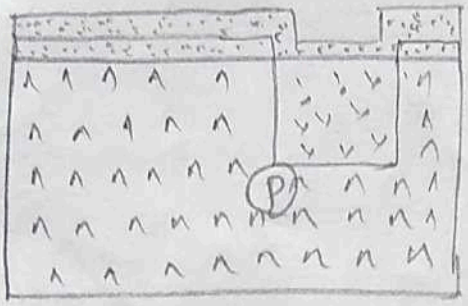
→ Wafer
→ doping with p-sub
→ deposite oxide layer

(2)



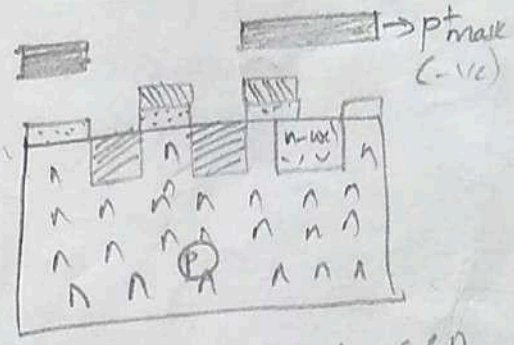
→ etching
→ n-diffusion

(3)



→ Again deposit oxide
→ Mask area for source & drain

(4)



→ Etching areas for S & D for both tx
→ Form gates by deposing polysilicon.

Technology :-

CMOS Fabrication steps

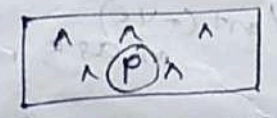
↳ 4-process

1. n-well 2. P-well 3. Twintub 4. SOI

N-well process :

CMOS → Nmos + Pmos

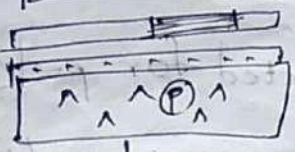
(S & D) + (S & D).

1) 

dope by P-sub.

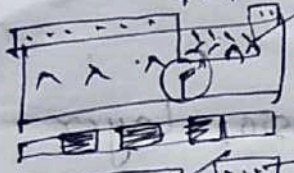
2) 

→ deposit oxide layer

3) 

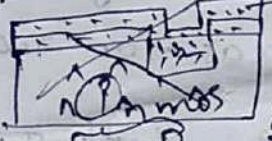
Wafer → doping with p-sub.

↳ Mask the well area

4) 

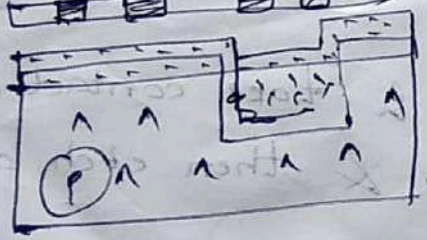
→ etching n-well area. (for P-mos S, D & G).

→ & diffuse by n-type for well.

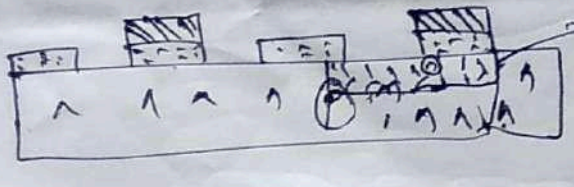
5) 

Again, deposit a thin layer of SiO_2, & mask areas for both Tx's (S, G, D & n-type S, G, D of p-type)

→ P-mos.



} photolithography

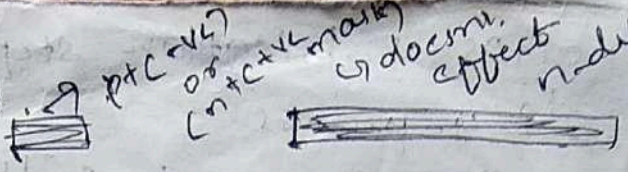
6) 

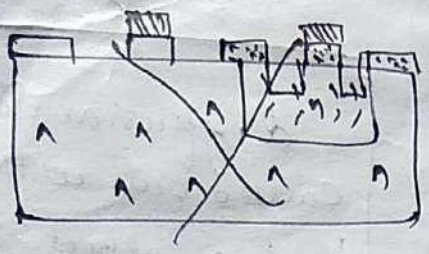
→ etching areas for S & D for both Tx's.

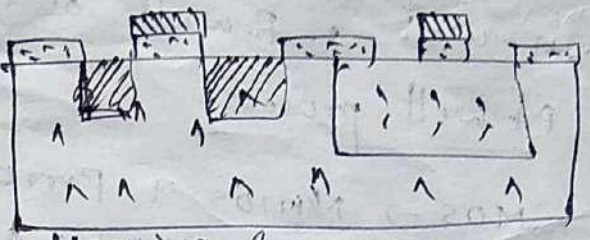
→ form gates by depositing polysilicon

Diffusion shud be carried out with care, doping affect V_T & breakdown volt

(7)

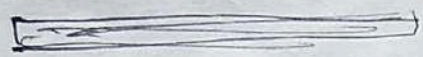




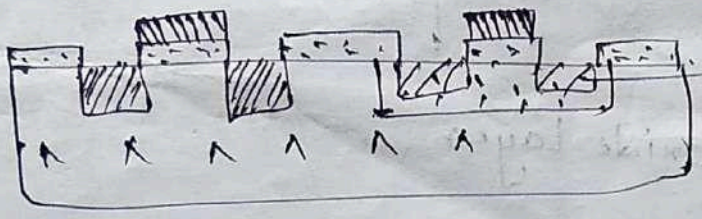


Masking & for diffusing n-type impurity for 'S' & 'D' of n-mos TX.

(8)



→ (p+(+ve) / n+(-ve)) mask.



→ p-diffusion for 'S' & 'D' of p-mos TX

or (n+ mask -ve)

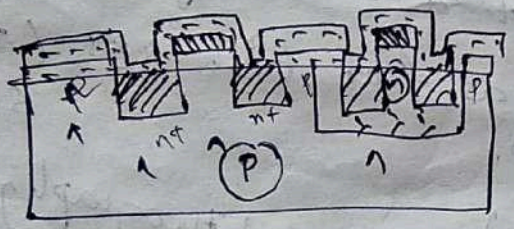
p+ mask (+ve) → masked area not effected for p-diff.

p+ mask (-ve) " " " " n-diffusion

or

n+ mask (+ve)

(9)



→ deposit SiO_2 layer.

→ mask areas for S, G, D for both Tx's.

→ Then etch the masked area & take contact cuts.

→ Finally deposit metal layer & then etch areas for contact cuts.

Bicmos Technology :-

→ Deficiency of MOS technology lies in the limited load driving capabilities, due to limited current sourcing & current sinking abilities.

→ Bipolar transistors + CMOS → Bi-cmos

→ Bi-cmos gates may be effective of speed in subsystem such as ALU, ROM etc.

Comparison between CMOS technology & Bi-polar technology

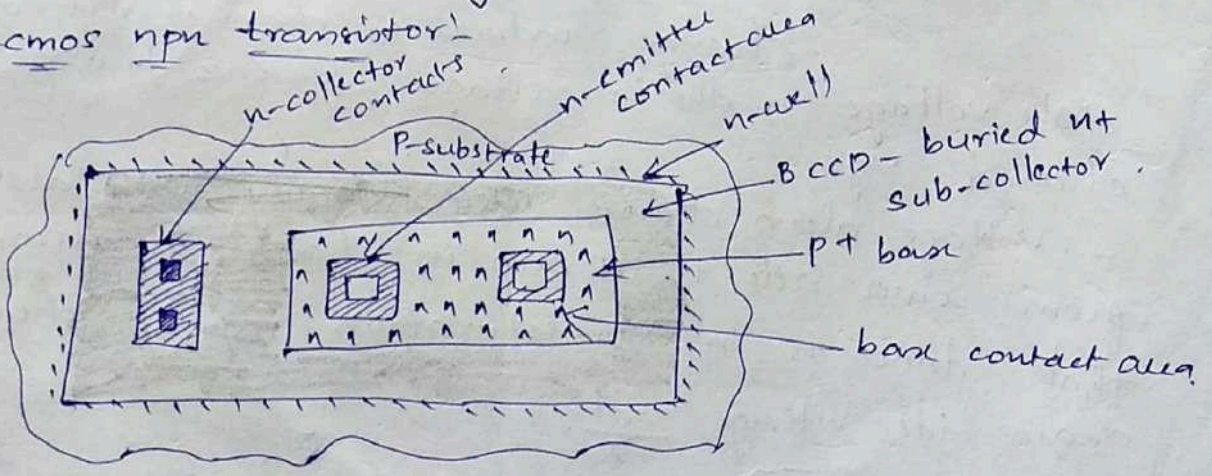
CMOS technology

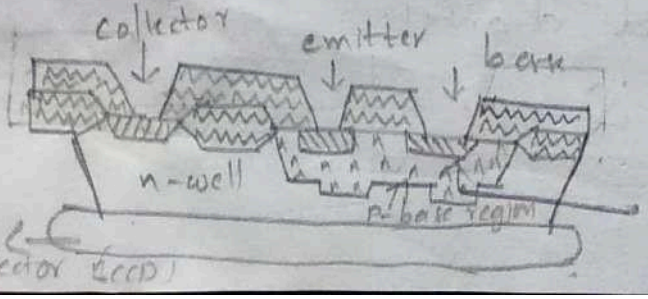
* Low static power dissipation
* High input impedance
* Scalable V_T
* High noise margin
* Low o/p drive I.
* Low gm
* Bi-directional capability

Bipolar technology.

* High Power dissipation
* Low i/p impedance.
* Low voltage swing logic.
* Low package density.
* High o/p drive 'I'.
* High gm.
* Unidirectional.

Bi-cmos npn transistor :-





Basic Electrical Properties of MOS & Bi-CMOS Circuits

DRAIN-TO-SOURCE CURRENT Ids Versus VOLTAGE Vds relationships

The MOS transistor evolves from use of voltage on the gate to induce charge in channel btwn source & drain. let vds applied between drain & source. since, charge induced is dependent on gate to source vgs & Ids is dependent on both vgs & vds.

Consider structure,

$$Ids = -Isd = \frac{Qc}{\tau}$$

$$\tau sd = L/v$$

$$Eds = \frac{Vds}{L}$$

$$v = \frac{\mu Vds}{L}$$

$$\tau sd = \frac{L^2}{Vds \cdot \mu}$$

$\mu n = 650\ cm^2/V\ sec$

$\mu p = 200\ cm^2/V\text{-}sec.$

$\Rightarrow$ Ids = -Isd = $\frac{\text{charge induced in channel (Q)}}{\text{Transit time } (\tau)}$.

Transit time $\Rightarrow \tau sd = \frac{\text{length of channel (L)}}{\text{velocity (v)}}$.

Velocity $v = \mu Eds$.

μ = mobility $cm^2/V\text{-}sec$

Non-saturated Region

charge induced in channel due to gate voltage is due to voltage difference b/w gate & channel, vgs.

→ voltage along channel varies linearly with distance from source due to IR drop in channel & assuming that device is in non-saturation region, then drain side voltage $\frac{Vds}{2}$.

Effective gate voltage (vg) = vgs − vt.

vt → voltage needed to invert charge under gate & established channel.

$$Q = cg \cdot v$$

Potential difference $V = \underbrace{V_{gs} - V_t}_{\text{Source}} - \underbrace{\frac{V_{ds}}{2}}_{\text{Drain}}$

$$C_g = \frac{\varepsilon_0 \varepsilon_r A}{D}$$

$$Q_c = \frac{\varepsilon_0 \varepsilon_r A}{D}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)$$

$$I_{ds} = \frac{Q_c}{T}$$

$$= \frac{\frac{\varepsilon_0 \varepsilon_r A}{D}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)}{\frac{L^2}{\mu V_{ds}}} \qquad (A = WL)$$

$$= \frac{\varepsilon_0 \varepsilon_r WL}{D} \times \frac{\mu V_{ds}}{L^2}\left((V_{gs} - V_t) - \frac{V_{ds}}{2}\right)$$

$$= \frac{\varepsilon_0 \varepsilon_r W}{D} \times \frac{\mu V_{ds}}{L}\left[(V_{gs} - V_t) - \frac{V_{ds}}{2}\right]$$

$$= \frac{\varepsilon_0 \varepsilon_r W}{DL} \cdot \mu\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right)$$

when $V_{ds} < V_{gs} - V_t$

Let $k = \frac{\varepsilon_0 \varepsilon_r \mu}{D}$

$$I_{ds} = \frac{kW}{L}\left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right]$$

Let $\beta = k \cdot \frac{W}{L}$

$$\therefore I_{ds} = \beta\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right)$$

$$k = \frac{\varepsilon_0 \varepsilon_r \mu}{D} \times \frac{A}{A}$$

Sub $k = \frac{\varepsilon_g \cdot \mu}{WL}$ in I_{ds}.

$$I_{ds} = \frac{C_g \mu}{WL} \cdot \frac{W}{L}\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right)$$

$$= \frac{C_g \mu}{L^2}\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right)$$

Gate Capacitance unit area C_0

$$C_0 = \frac{C_g}{WL} \Rightarrow C_g = C_0 \cdot WL$$

$$\therefore I_{ds} = \frac{C_0 \mu W}{L}\left((V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2}\right)$$

Saturation Region:-

$$V_{ds} = V_{gs} - V_t$$

$$I_{ds} = \beta\left[(V_{gs}-V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$$= \beta\left(V_{ds}.V_{ds} - \frac{V_{ds}^2}{2}\right)$$

$$= \beta\left(\frac{V_{ds}^2}{2}\right)$$

$$\boxed{I_{ds} = \frac{\beta}{2}(V_{gs}-V_t)^2}$$

$$\boxed{I_{ds} = \frac{C_{ox}\mu}{2}\left(\frac{W}{L}\right)\left(\frac{V_{ds}^2}{2}\right)}$$

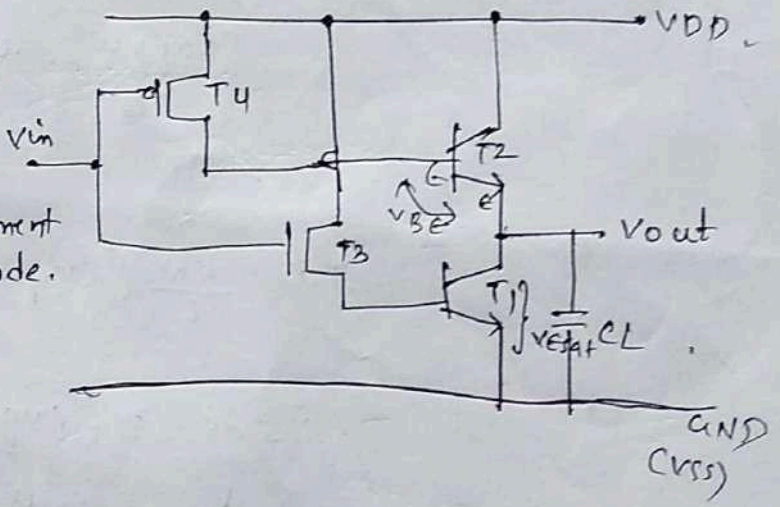
$$\boxed{I_{ds} = \frac{C_{ox}\mu W}{2L}(V_{gs}-V_t)^2}$$

for both Enhancement & depletion mode.

BiCMOS Inverter

→ It consists of 2 Bi-polar transistors T_1, T_2.

and 1 nmos Tx – T_3
1 pmos Tx – T_4 } Enhancement mode.



Case 1: Logic 0 i/p.

$V_{in} = 0$ (VSS)

$T_3 \rightarrow$ off & T_4 – ON

As T_3 – off, T_1 will be non-conducting mode.

→ T_4 is on & supplies 'I' to the base of 'T_2', which will conduct & act as a I-source to charge the load C_L toward +5V (VDD).

The o/p of inverter will rise to +5V. Less, the base to emitter voltage V_{BE} of T_2 i.e VBB

$$\boxed{V_{DD} - V_{BE} = \text{Logic 1}}$$

Case 2: With V_{in} = +5V (VDD)

$T_4 \rightarrow$ off, so that T_2 is non-conducting

T_3 is on & will Supply 'I' to the base of T_1, which will

conduct & act as a I-sink to load C_L, discharging towaid 0V.

(2). Voltage V_{CEsat} from collector to emitter of T_1 i.e

$$0V + V_{CEsat} = \text{logic } 0.$$

→ T_1 & T_2 will present low impedances when turned on into Saturation & load C_L will be charged or discharged Rapidly.

→ The o/p logic levels will be good & will be close to Rail voltages. Since, V_{CEsat} is small & $V_{BE} \cong 0.7V$ (V_{OL}, V_{SS})

$$(V_{SS})_0 \cong V_{CEsat}; \quad 5 - 0.7 \cong V_{DD}$$

→ The inverter has high i/p impedance.

→ The inverter has low o/p impedance.

→ The inverter has high noise margins.

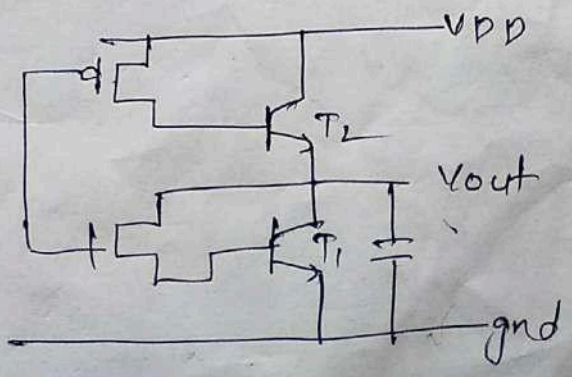
→ Due to the presence of a DC path from V_{DD} to GND through T_3 & T_1, this is not a good arrangement to implement since there will be significant static 'I' flow whenever V_{in} = logic 1.

→ Disadvantage:- No discharge path for 'I' from base of BJT, when it is being turned off. So, that circuit slows down.

To avoid this,

* DC path through T_3 & T_1 Eliminated.
* o/p V-swing ↓d.

Improved Inverter Arrangement with resistors



Latchup in CMOS circuits

2.3 MOS Transistor Transconductance g_m & d_p conductance g_{ds} (1)

Transconductance expresses relation between o/p current I_{ds} & i/p voltage v_{gs}

$$g_m = \frac{\delta I_{ds}}{\delta v_{gs}} \Big| v_{ds} = \text{constant}$$

→ small change in v; large change in I

Consider charge in channel Q_c

$$\frac{Q_c}{I_{ds}} = \tau \qquad (\because I_{ds} = \frac{Q_c}{\tau})$$

Where, Transit time 'τ' is

change in $I \rightarrow$ $\delta I_{ds} = \frac{\delta Q_c}{\tau_{ds}}$ $\qquad (\because \tau_{ds} = \frac{L^2}{\mu v_{ds}})$

change in charge, $\qquad (\because Q = CV)$.

$$\delta Q_c = C_g \cdot \delta v_{gs}$$

$$\delta I_{ds} = \frac{C_g \cdot \delta v_{gs}}{\tau_{ds}}$$

$(\because Q = CV)$

Camount of charge moves into plate, depends on 'c' & V).

$$= \frac{C_g \delta v_{gs}}{\frac{L^2}{\mu v_{ds}}} = \frac{C_g \delta v_{gs} \mu v_{ds}}{L^2}$$

Now,

$$g_m = \frac{\delta I_{ds}}{\delta v_{gs}} = \frac{C_g \mu v_{ds}}{L^2}$$

i.e $= \frac{C_g \delta v_{gs} \mu v_{ds}}{L^2 \times \delta v_{gs}}$

In sat regim. $v_{ds} = v_{gs} - v_t$.

$$g_m = \frac{C_g \mu}{L^2} (v_{gs} - v_t).$$

$$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0}{D} \frac{W}{L} (v_{gs} - v_t) \qquad (\because C_g = \frac{\varepsilon_{ins} \varepsilon_0 WL}{D})$$

(4) $g_m = \beta(V_{gs} - V_t)$.

o/p conductance, g_{ds} can be expressed as

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{gs}}$$

$$= \lambda I_{ds} \propto \left(\frac{1}{L}\right)^2.$$

Figure of merit ω_0:- is a quantity used to characterise performance of device / system.

$$\omega_0 = \frac{g_m}{C_g} = \frac{\mu}{L^2}(V_{gs} - V_t)$$

$$= \frac{1}{T_{sd}}.$$

$g_m = \frac{\mu \varepsilon_{ins} \varepsilon_0 W}{D \cdot L}(V_{gs} - V_t)$

$\omega_0 = \frac{\mu \varepsilon_{ins} \varepsilon_0 W (V_{gs} - V_t)}{DL} \Big/ \frac{\varepsilon_{ins} \varepsilon_0 WL}{D}$

$C_g = \frac{\varepsilon_{ins} \varepsilon_0 WL}{D}$

$= \frac{\mu (V_{gs} - V_t)}{L^2}$ ✓

Hence, it is seen that switching speed depends on gate voltage & inversely on the square of length.

Pass Transistor :-

Unlike bipolar Tx's, isolated nature of gate allows Mos Tx's used as switches in series with lines carrying logic levels in a way i.e similar to use of relay contacts. This application is called the "pass transistor."

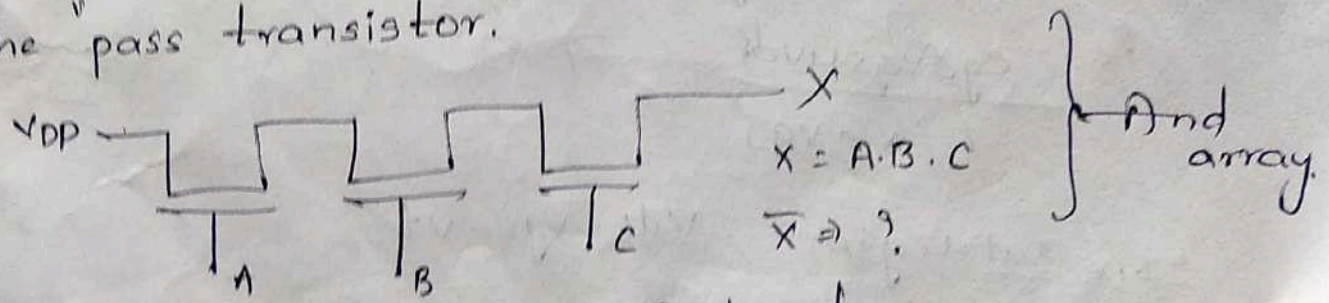


fig. Pass Tx And gate.

→ It reduces count of Tx's, by eliminating redundant Tx's.

N-mos Inverter

The basic inverter circuit requires a Tx with source connected to ground & a load of Rx of some sort connected from drain to positive supply rail VDD.

logic 1 = +5V
0 = 0V

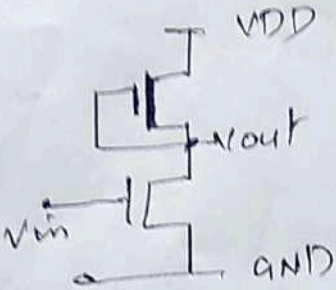


fig: nmos inverter.

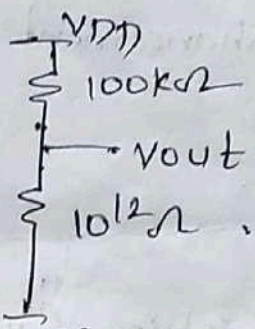
Depletion Tx
always 'ON' state.
Vgs = 0V.

When Vin = 0V.

Enhancement Tx → OFF.

Vout = 5V = logic 1.

ID = 0; open circuit, Vout = 1



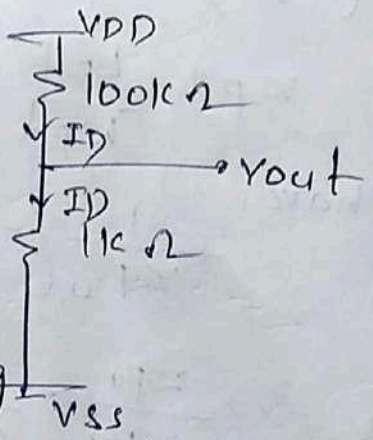
When Vin = 1V

Tx = ON.

Vgs

→ ID flows

→ Apply v-dividing rule.



$$V_{out} = \frac{R_2}{R_1 + R_2} \times V_{in}$$

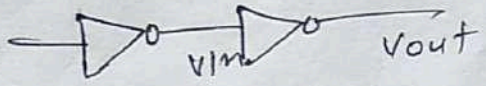
$$= \frac{1k}{1k + 100k} \times 5V$$

$$V_{out} \simeq 0V$$

Determination of PULL-UP to PULL-DOWN RATIO (z_{pu}/z_{pd}) for an N-mos inverter driven by another nmos

Let's consider depletion mode Tx for which

$V_{gs}=0$, $V_{in}=V_{out}=V_{inv}$.



Let us set $V_{in}=0.5V_{DD}$

$$I_{ds}=k\frac{W}{L}(V_{gs}-V_t)^2$$

In depletion mode,

$$I_{ds}=K\cdot\frac{W_{p.u}}{L_{p.u}}\frac{(-V_{td})^2}{2} \quad (\because V_{gs}=0)$$

Enhancement mode,

$$I_{ds}=k\cdot\frac{W_{p.d}}{L_{p.d}}\frac{(V_{in}-V_t)^2}{2} \quad (\because V_{gs}=V_{in})$$

Let equate currents.

$$\frac{\text{width}}{\text{length}}\Big|_{\text{of pullup \& down}}\left(\frac{-V_{td}}{2}\right)^2=\frac{W_{pd}}{L_{pd}}\frac{(V_{in}-V_t)^2}{2}$$

Now, $z_{p.d}=\frac{L_{p.d}}{W_{p.d}}$ $\quad z_{pu}=\frac{L_{pu}}{W_{p.u}}$

We have, $$\frac{1}{z_{p.u}}(-V_{td})^2=\frac{1}{z_{pd}}(V_{in}-V_t)^2$$

$$\frac{z_{pu}}{z_{pd}}=\frac{(V_{td})^2}{(V_{in}-V_t)^2}$$

Now substitute with standard typical values

$V_t=0.2V_{DD}$; $V_{td}=-0.6V_{DD}$, $V_{inv}=0.5V_{DD}$

$$\frac{z_{pu}}{z_{pd}}=\frac{(-0.6V_{DD})^2}{((0.5-0.2)V_{DD})^2}=\frac{0.6\times0.6}{0.3\times0.3}=\frac{4}{1}$$

$$\boxed{\frac{z_{pu}}{z_p}=\frac{4}{1}}$$

Pull up to pull down ratio for N-mos inverter driven through one or more pass Transistor

The i/p to inverter 2 comes from o/p of inverter 1 but passes through 1 or more n-mos transistors used as switches in series called pass transistors

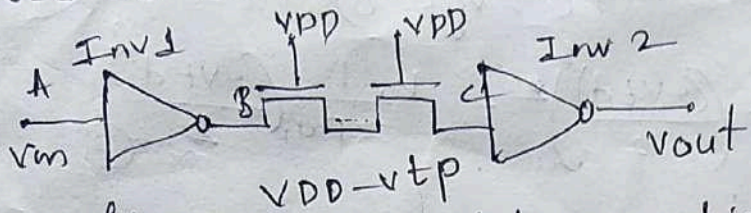


fig. Pullup to pull down ratio for inverting logic by pass Tx

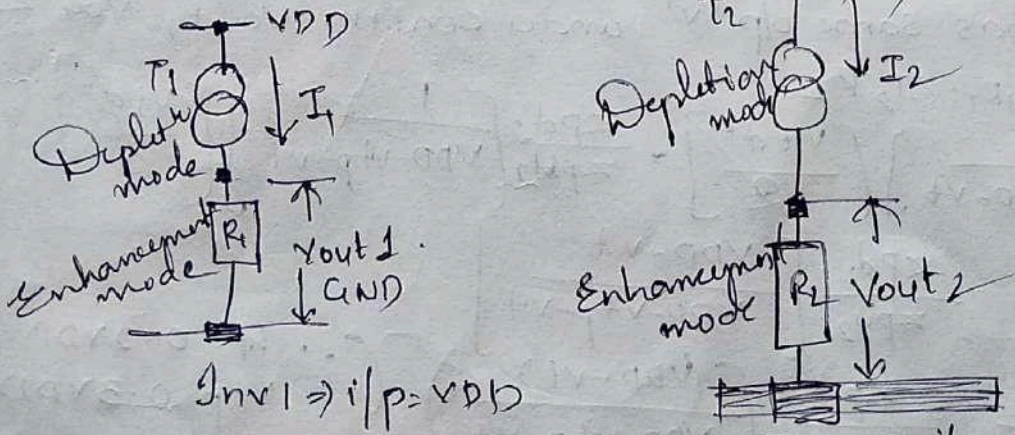
→ With all pass tx gates connected to VDD, in series, no static 'I' flows through them & no voltage drop in channels.

i/p voltage at inv 1 = Vin

inv 2 = VDD − Vtp
↳ pass Tx V_T

consider Inv 1, i/p = VDD, then the P.d Tx T_2 is conducting but with low 'V', & represented by R_1 (& in resistive region)

P.u Tx is in satuation region



For P.d Tx,

$$I_{ds} = k \cdot \frac{W_{pd}}{L_{pd}} \left((V_{DD} - V_t) V_{ds1} - \frac{V_{ds1}^2}{2} \right)$$

$$\therefore R_1 = \frac{V_{ds1}}{I_{ds}} = \frac{V_{ds}}{K \cdot \frac{W_{pd1}}{L_{pd1}} \left[(V_{DD} - V_t) - \frac{V_{ds1}}{2} \right] \times V_{ds}}$$

Note v_{ds_1} is small & $v_{ds_1}/2$ is ignored

$$R_1 = \frac{1}{K} \frac{L_{pd_1}}{W_{pd_1}} \left[\frac{1}{V_{DD} - V_t - \frac{v_{ds_1}}{2}} \right]$$

$$R_1 = \frac{1}{K} z_{pd_1} \left[\frac{1}{V_{DD} - V_t} \right] \rightarrow (1) \quad (\because z = \frac{L}{W})$$

Now for depletⁿ mode p.u in saturation

$\hookrightarrow (\because v_{gs} = 0)$

$$I_1 = I_{ds} = K \cdot \frac{W_{pu_1}}{L_{pu_1}} \left(\frac{(-V_t - d)}{2} \right)^2 = K \cdot \frac{1}{z_{pu_1}} \left(\frac{-V_t - d}{2} \right)^2 \rightarrow (2)$$

We know, $I_1 R_1 = V_{out_1}$

$$\boxed{V_{out\,1} = I_1 R_1 = \frac{z_{pd_1}}{z_{pu_1}} \left[\frac{1}{V_{DD} - V_t} \right] \left[\frac{V_t - d}{2} \right]^2}$$

Consider Inverter 2:

When $i/p = V_{DD} - V_{tp}$.

From eqⁿ (1) inv 1 $\rightarrow R_2 = \frac{1}{K} z_{pd_2} \left[\frac{1}{(V_{DD} - V_{tp}) - V_t} \right]$ ($\because \frac{v_{ds_1}}{2}$ was neglected)

(i/p of inv_2)

From eqⁿ (2) $I_2 = K \frac{1}{z_{pu_2}} \left(\frac{V_t - d}{2} \right)^2$

Hence,

$$\boxed{V_{out\,2} = I_2 R_2 = \frac{z_{pd_2}}{z_{pu_2}} \left[\frac{1}{V_{DD} - V_{tp} - V_t} \right] \left[\frac{V_t - d}{2} \right]^2}$$

If inv-2 has same o/p 'v'; under conditns $V_{out_1} = V_{out_2}$

$$I_1 R_1 = I_2 R_2$$

$$\therefore \frac{z_{pd_1}}{z_{pu_1}} \left[\frac{1}{V_{DD} - V_t} \right] \left[\frac{V_t - d}{2} \right]^2 = \frac{z_{pd_2}}{z_{pu_2}} \left[\frac{1}{V_{DD} - V_{tp} - V_t} \right] \left[\frac{V_t - d}{2} \right]^2$$

$$\frac{z_{pd_1}}{z_{pu_1}} = \frac{z_{pd_2}}{z_{pu_2}} \left[\frac{V_{DD} - V_t}{V_{DD} - V_{tp} - V_t} \right]$$

$$\frac{z_{pu_2}}{z_{pu_1}} = \frac{z_{pd_2}}{z_{pd_1}} \left[\frac{(V_{DD} - V_t)}{V_{DD} - V_{tp} - V_t} \right] \quad (\because V_t = 0.2 V_{DD}, \; V_{tp} = 0.3 V_{DD})$$

$$= \left[\frac{V_{DD} - 0.2 V_{DD}}{V_{DD} - 0.3 V_{DD} - 0.2 V_{DD}} \right] = \frac{0.8}{0.5}$$

$$\frac{z_{pu_2}}{z_{pu_1}} = \frac{z_{pd_2}}{z_{pd_1}} \left[\frac{0.8}{0.5} \right]$$

$$= \simeq \frac{8}{1}$$

Alternative Forms of Pullup

↳ 4 possible Arrangements.

1. Load Resistance R_L :- This is not often used because of large space requirements of resistor produced in silicon substrate.

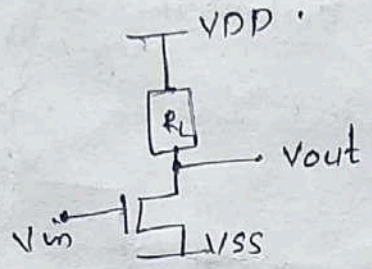
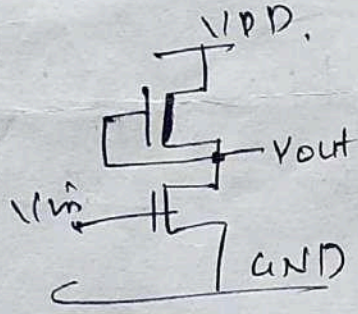


fig. Resistor Pull-up.

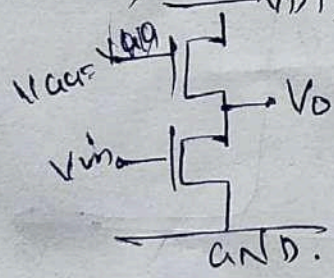
2. n-mos depletion mode Tx pull-up'.

a) dissipation is high.
b) switching of o/p from 1 to 0 begin when Vin exceeds Vt of Pulldown device.

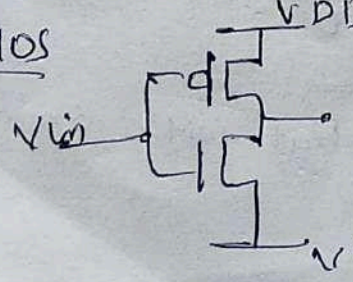


3). nmos Enhancement mode : (Pull-up).

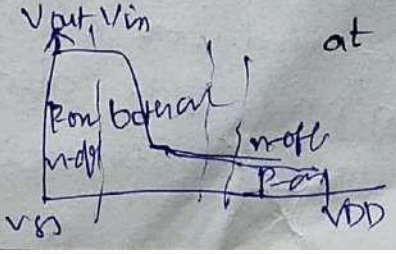
a) Dissipation is high.
b) Vout can never reach VDD, if Vaa = VDD.
c) if Vaa > VDD; extra supply of rail is required



4) CMOS



a) Full Logical Levels 1 & 0 are presented at o/p.



CMOS Inverter

The I/V relation for Mos Tx may be

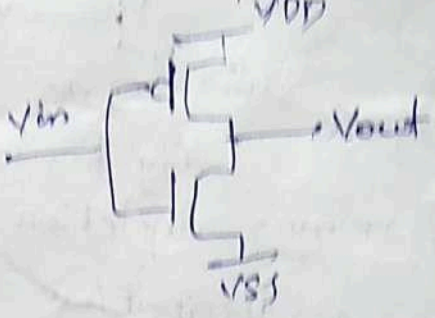
$$I_{ds} = k\frac{W}{L}\left(v_{gs}-v_t\right)v_{ds} - \frac{v_{ds}^2}{2} \quad \text{(non-sat)}$$

or

$$I_{ds} = \frac{k\cdot W}{L}\frac{(v_{gs}-v_t)^2}{2} \quad \text{(saturation region)}$$

'k' is technologically dependent factor (parameter)

$$k = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}$$



$$\beta = \frac{k\cdot W}{L}$$

$$I_{ds} = \frac{\beta}{2}(v_{gs}-v_t)^2$$

In saturation, 'β' may be applied to both nmos & Pmos Tx

$$\beta_n = \frac{\varepsilon_{ins}\varepsilon_0\mu_n}{D}\frac{W_n}{L_n} \quad ; \quad \beta_p = \frac{\varepsilon_{ins}\varepsilon_0\mu_p}{D}\frac{W_p}{L_p}$$

Let's consider the condition for region 1 for which Vin = '0'.

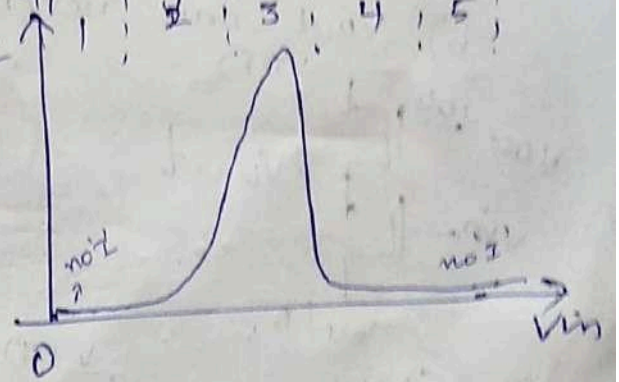
So, P-Tx → ON ; N-Tx → OFF.

Thus, no current flows through inverter & o/p is directly connected to VDD. o/p = Logic 1

→ In region 5; Vin = Logic 1;

n-Tx is on, P is OFF. no 'I' flows, & o/p = Logic '0'.

→ In region 2, i/p 'v' ↑ & exceeds V_T of n-Tx.



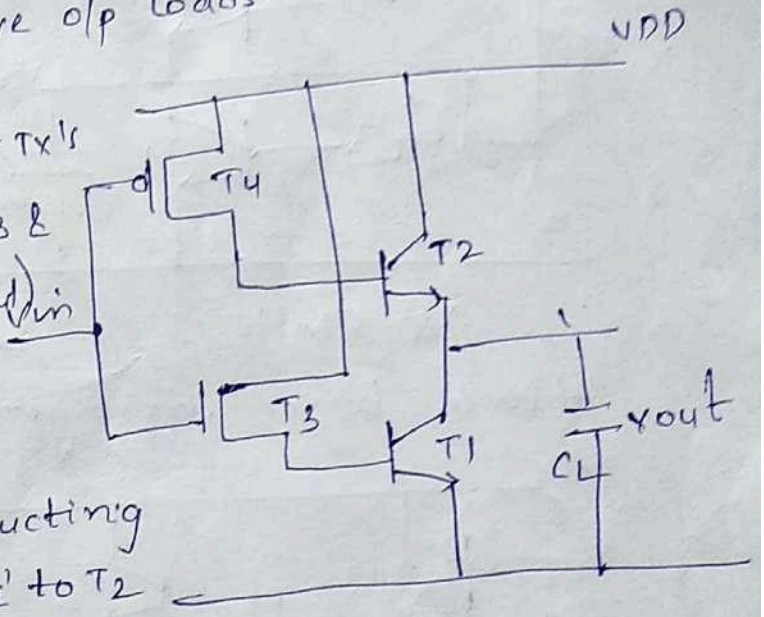
p-Tx conducts & in saturation region. N-Tx also conducts but with small voltage & in resistive region.

Region-4 Ilar to Region '3', roles of p & n are reverse
Region-3; inverter exhibits gain & both Tx's are in saturation region.

Bi-CMOS Inverters

BiCMOS — The logical approach in designing includes

(i) MOS Tx - Performs Logic functions
2). Bipolar Tx - drive o/p loads.



→ It consists of 2 bipolar Tx's T_1 and T_2 & 1 Nmos Tx T_3 & 1 p-mos Tx T_4 (Enhancement)

→ Vin=0; → T_3 = OFF
↓
T_1 → non-conducting
T_4 → ON & supplies 'I' to T_2 which conducts & act as 'I' source & charge C_L (+5V)

Vout = 5V; Logic 1.

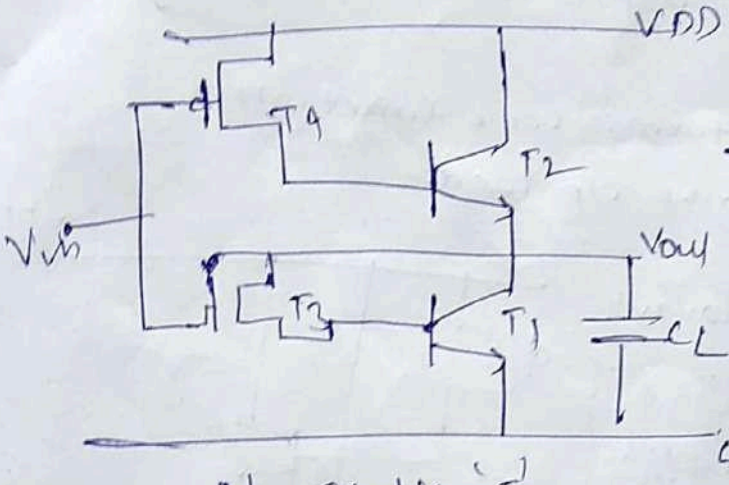
→ Vin = 5V; T_4 → OFF → T_2 is non-conducting.
T_3 → OFF → T_1 conducts & discharge load C_L (0V).

Vout = 0V; Logic '0'.

* Inverter has
(i) high i/p impedance
2) Low o/p "
3) high noise margin
4) small area
5) High driving capability

Hence, direct presence of DC path from VDD to GND through T_3 & T_1 is not a good arrangement & can lead to static I-flow.

Improvised version.

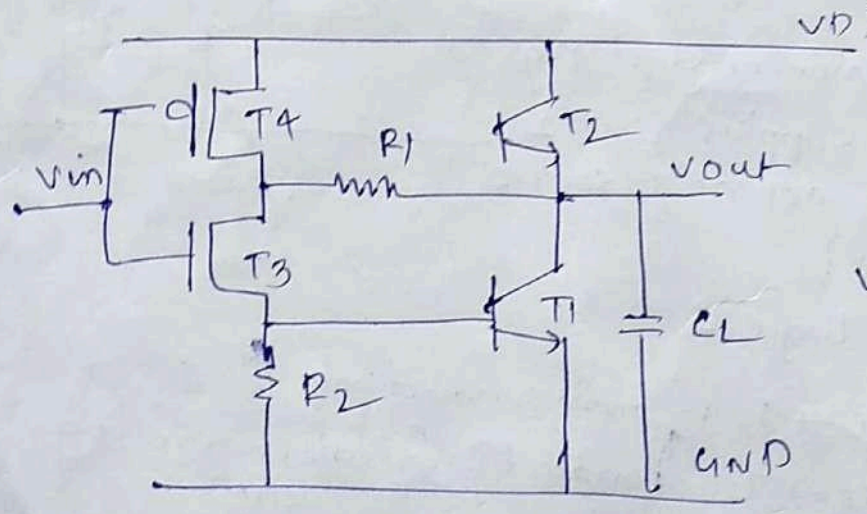


→ direct path reduced

→ Hence voltage o/p swing ↓.

No static 'I'.

Hence better arrangement using Rx.



Voltage o/p swing ↑.