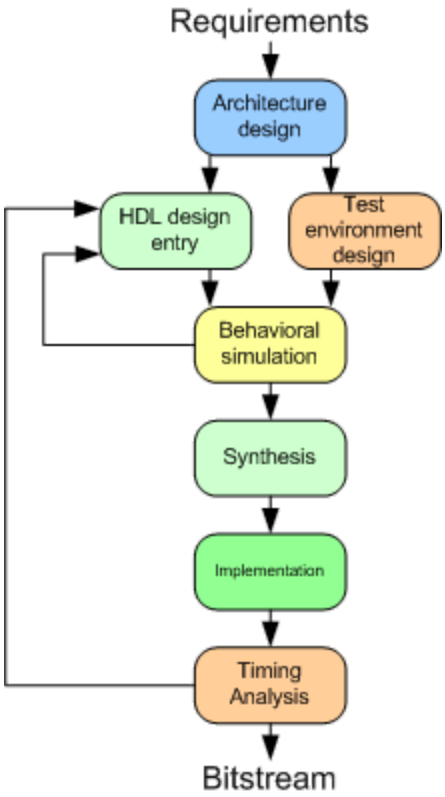
FPGA design Flow :



1) Architecture design. This stage involves analysis of the project requirements, problem decomposition and functional simulation (if applicable). The output of this stage is a document which describes the future device architecture, structural blocks, their functions and interfaces.

2) HDL design entry. The device is described in a formal **hardware description language (HDL)**. The most common HDLs are VHDL and Verilog.

3) Test environment design. This stage involves writing of test environments and behavioral models (when applicable). They are later used to ensure that the HDL description of a device is correct.

4) Behavioral simulation. This is an important stage that checks HDL correctness by comparing outputs of the HDL model and the behavioral model (being put in the same conditions).

5) Synthesis. This stage involves conversion of an HDL description to a so-called *netlist* which is basically a formally written digital circuit schematic. Synthesis is performed by a special software called *synthesizer*. For an HDL code that is correctly written and simulated, synthesis shouldn't be any problem. However, synthesis can reveal some problems and potential errors that can't be found using behavioral simulation, so, an FPGA engineer should pay attention to warnings produced by the synthesizer.

6) Implementation. A synthesizer-generated netlist is mapped onto particular device's internal structure. The main phase of the implementation stage is *place and route* or *layout*, which allocates FPGA resources (such as logic cells and connection wires). Then these configuration data are written to a special file by a program called *bitstream generator*.
7) Timing analysis. During the timing analysis special software checks whether the implemented design satisfies timing constraints (such as clock frequency) specified by the user.

Read more: **http://www.fpgacentral.com/docs/fpga-tutorial/fpga-design-flow-overview#ixzz2XoZeTUxl**

Xilinx ISE installation:

1) Register at xilinx website http://www.xilinx.com

2) Download a version that supports your operating system : http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools.html

3) Obtain a licence, it will be sent to your email
https://xilinx.entitlenow.com/AcrossUser/main.gsp?licenseType=&product=&tab=CreateLicense&

4) Follow the document downloaded with the tool to install according to your operating system.

5) During installation select to install ISE:web pack (because it' licence is free)

6) when asked for the licence, point to your downloaded licence file

7) Set the environmental variables: this is best explained in this document:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/iil.pdf

More illustrative document (Follow the EE101 students path) :
http://www-classes.usc.edu/engr/ee-s/201/Spring2012/ISE/ISE_13.2_Installation_steps_USC.pdf