Roll No…….. **Total No. of Printed Pages: [01]**

Total No. of Questions: [09]

B. Tech. (ECE) (Semester – 3rd)

DIGITAL ELECTRONIC CIRCUITS & DESIGN

Subject Code: BECES1-302

Paper ID: [18111311]

Time: 03 Hours **Maximum Marks: 60**

Instruction for candidates:

1. Section A is compulsory. It consists of 10 parts of two marks each.
2. Section B consist of 5 questions of 5 marks each. The student has to attempt any 4 questions.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

Section – A **(2 marks each)**

Q1. Attempt the following:

a) Why XNOR gate is called an Equivalence gate? Find its output (in Hex), if inputs given to a 2-input XNOR gate are A1 and C2 respectively.

b) Realize the truth table for the Boolean function: $F = A.\overline{B.C} + \overline{A}.C + \overline{C}.D$

c) Illustrate OR and NOR gates using NAND gates only.

d) Differentiate between working of PAL and PLA.

e) Realize a 4:1 Multiplexer using 2:1 Multiplexers.

f) Exhibit a fully labelled SR NOR latch with Preset and Clear facility.

g) Distinguish between Active HIGH and Active LOW digital circuits.

h) Compare various performance characteristics of TTL and MOS logic family.

i) Illustrate Absorption Theorem along with its Dual.

j) Compare and contrast Moore and Mealy model-based machines.

Section – B **(5 marks each)**

Q2. Demonstrate the working of a 4-bit SIPO and PISO type of Shift Registers.

Q3. Convert $F = \overline{B} + \overline{A}.\overline{B}.\overline{C} + \overline{C}$ into Canonical SOP and implement with NAND gates only.

Q4. Implement a full Adder using i) Multiplexers, ii) Decoders only.

Q5. Illustrate the working of an edge triggered JK Flip Flop with the help of Truth table, Excitation table, Characteristic equation and State Transition diagram.

Q6. Realize a 4-bit Magnitude Comparator to show that a number A is either greater than or equal to B i.e. ($A \geq B$).

Section – C **(10 marks each)**

Q7. Minimize the Boolean expression $Z = \sum (3, 5, 6, 11, 12, 15) + d(0, 1, 7, 13)$ using Karnaugh Map and implement both original and simplified circuits using 2-inputs NAND gates only. Find the percentage saving achieved.

Q8. What is a synchronous counter? Design a modulo-10 up-down Counter using Flip Flops.

Q9. Write a complete technical note on *any two* of the following:

i) Gray Codes: its properties and applications
ii) FPGA
iii) Finite State machines: its capabilities and limitations.