**Computer Organization and Architecture and Lab (CS2600, CS2610)**
**Jan - May 2024**

**Schedule**

**references:**
**[COD] Computer Organization and Design, RISC V Edition, Patterson and Hennessey**
**[RISCV-PI]RISC V ISA - Privileged Instructions**
**[MPD] Modern Processor Design - Shen and Lipasti**

| Sl | Date | Topic |
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| 01 | 2024-01-17 (W) | **Introduction**<br>Introduction to the course |
| 02 | 2024-01-23 (Tu) | **Instruction Set Architecture support for Programming Languages**<br>**REF. [COD Ch 2]**<br>Stored program concept; Von Neumann Bottleneck; Compiler assembler and linker |
| 03 | 2024-01-24 (W) | Opcodes, Instructions,Registers,and RISC V |
| 04 | 2024-01-29 (M) | R type, I type instructions. Load and Store instructions in RISC V |
| 05 | 2024-01-29 (M) | **LAB 1:** Cross compilers for RISC V; SPIKE; simple assembly program |
| 06 | 2024-01-30 (Tu) | R type, I type Instructions, Load and Store instructions of RISC V. Aligned and Non-aligned memory accesses. |
| 07 | 2024-01-31 (W) | First assembly program (strlen); ELF executables; linker scripts |
| 08 | 2024-02-02 (Fr) | **Tutorial 1:** RISC V assembly programming -- a review |
| 09 | 2024-02-05 (M) | executing the program; on hardware vs spike; support for function calls |
| 10 | 2024-02-05 (M) | **LAB 2:** Multi-precision arithmetic in RISC V |
| 11 | 2024-02-06 (Tu) | support for function calls; parameter passing, stack frames, return values, caller and callee saved registers |
| 12 | 2024-02-07 (W) | **Building a simple single cycle RISC V processor.**<br>**Ref. [COD Ch 4]**<br><br>Program Counter, Control Unit, R-type instructions |
| 13 | 2024-02-09 (Fr) | **Class Test 2:** RISC V assembly |
| 14 | 2024-02-12 (M) | I type instructions, Load and Store instructions of RISC V. |

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| 15 | 2024-02-12 (M) | **LAB 3:** Stack and Recursion |
| XX | 2024-02-13 (Tu) | class shifted to 2024-02-23 |
| 16 | 2024-02-14 (W) | Memory mapped peripherals. Polling to communicate with peripherals. |
| 17 | 2024-02-16 (Fr) | Discussion on Tutorial 2. |
| 18 | 2024-02-19 (M) | Memory mapped peripherals, interrupts, RISC V's CLINT and PLIC, multi-tasking environments with timer interrupts |
| | 2024-02-19 (M) | No lab today due to quiz week |
| 19 | 2024-02-20 (Tu) | Multi-tasking environments and Direct memory access<br>**Instruction Set Architecture support for Operating Systems**<br>**Ref. [COD 5] [RISCV-PI]**<br>Control Status Registers (CSRs); Privilege modes -- Machine, Supervisor, User. |
| 20 | 2024-02-21 (W) | Quiz 1 |
| 21 | 2024-02-23 (Fr) | Interrupt handling in RISC V; mcause; mstatus; CSRs |
| 22 | 2024-02-26 (M) | Nested interrupts, multitasking with interrupts, interrupt pending and enable. |
| 23 | 2024-02-26 (M) | **Lab 4:** ABI Assembly and C interaction |
| 24 | 2024-02-27 (Tu) | Multi-tasking with virtual memory. General concept. PTBR. page frames, page blocks. swap space |
| 25 | 2024-02-28 (W) | two level-page translation. satp. csrs and formats of page frame, page table entry etc. in RISC V |
| 26 | 2024-02-30 (Fr) | Quiz 1 discussion |
| 27 | 2024-03-04 (M) | Three level-page translation in RISC V. |
| 28 | 2024-03-04 (M) | **Lab 5:** Switching between Supervisor and Machine mode; Timer interrupt handling |
| 29 | 2024-03-05 (Tu) | **The Memory Hierarchy.**<br><br>**Ref. [COD Ch5]**<br>DRAM Organization. Ranks, Chips, Rows, Columns, Arrays, Banks, memory controller. |
| 30 | 2024-03-06 (W) | DRAM addressing, Burst mode, Interleaved mode, |
| 31 | 2024-03-11 (M) | **Class Test 3:** up to virtual memory (Virtual memory) |
| 32 | 2024-03-11 (M) | **Lab 6:** Multi-tasking environments in RISC V |
| 32 | 2024-03-12 (Tu) | DRAM Refresh; Cache memories, SRAM vs DRAM, hierarchy |

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| 33 | 2024-03-13 (W) | Direct Mapped Caches, Mapping, Tags, |
| 34 | 2024-03-15 (Fr) | Write back, Write through caches. Write miss using write allocate |
| 35 | 2024-03-18 (M) | Fully associative and set-associative cache memory |
| 36 | 2024-03-19 (Tu) | Virtual memory and caches (PIPT, VIVT, VIPT), split and unified cache memory |
| 37 | 2024-03-20 (W) | **Quiz 2** |
| 38 | 2024-03-22 (Fr) | Virtual memory lab assignment discussion |
| 39 | 2024-03-26 (Tu) | Cache Performance<br><br>**CPU Pipelines.** Stages; Hazards; gains by pipelines. Structural Hazards **Ref. [COD Ch4.7 onwards]** |
| 40 | 2024-03-27 (W) | Data hazards; reordering instructions, forwarding; Control hazards. Assume not taken. |
| 41 | 2024-03-01 (M) | Branch predictors, Performance of Scalar Pipelines **[MOD Ch 3]** |
| 42 | 2024-04-01 (M) | **Lab 7:** Virtual Memory in RISC V |
| 43 | 2024-04-02 (Tu) | **Superscalar Organization** **Ref [MPD Ch 4.]**<br>Scalar pipelines/Parallel pipelines/diversified pipelines<br>N-issue pipelines |
| 44 | 2024-04-03 (W) | multi-entry reorder buffers, out-of-order execution |
| 45 | 2024-04-05 (Fr) | Quiz 2 paper discussion<br>**Lab 8:** Pipelined processor in C++ |
| 46 | 2024-04-08 (M) | The superscalar pipeline stages; Instruction Fetch, Decode, Dispatch |
| 47 | 2024-04-10 (W) | Execution, Completion, Retire. Example of an instruction flow |
| 48 | 2024-04-12 (Fr) | Lab 9 explanation;<br>Exception handling; branch handling; speculation |
| 49 | 2024-04-15 (M) | Handling RAW, WAW, WAR. Register renaming |
| 50 | 2024-04-16 (Tu) | More on register renaming; Using virtual registers. |
| 51 | 2024-04-17 (W) | Example of instruction flow in a superscalar pipeline with register renaming |
| 52 | 2024-04-22 (M) | **Class Test 5:** Cache Memories |
| 53 | 2024-04-24 (W) | **Multithreading and Multicore.** Symmetrical, Fine-grained, Course-grained Multithreading (Dr. Gopalakrishnan Srinivasan) |

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| 54 | 2024-04-29 (M) | Multi-core processors (Arjun Menon, Incore Semiconductors) |
| 55 | 2024-04-30 (Tu) | Multi-core processors (Arjun Menon, Incore Semiconductors) |
| 56 | 2024-05-01 (W) | Multi-core processors (Arjun Menon, Incore Semiconductors) |
| 57 | 2024-05-03 (Fr) | **Class Test 6:** Scalar and superscalar processors |
| 58 | 2024-05-09 | Final Exam |