FX2 FIFO Interface

External Master

Synchronous

Register	Purpose	FX2 Loopback External Master	FIFO Slave
FIFOADD0	LSB of endpoint FIFO that is active	PA4	PA4
FIFOADD1	MSB of endpoint FIFO that is active	PA5	PA5
FD[7:0] (FIFO_DATAPORT_LOW)	LSB of data to be sent	IOB/Port B	IOB/Port B
FD[15:8] (FIFO_DATAPORT_HIGH)	MSB of data to be sent	IOD/Port D	IOD/Port D
FF	Full Flag sent from slave to master	CTL2/FLAG B	CTL2/FLAG B
PKTEND	Signal early packet end	PA6	PA6
SLWR	Write to slave	PA3	RDY1/SLWR
IFCLK	Clock Sync	IFCLK	IFCLK

Synchronous Write

In theory this should work, still a WIP. Reference:
http://www.cypress.com/file/126446/download#G12.1129884

// 11 is ep8
IFCLK = 1
FIFOADD0 = 1
FIFOADD1 = 1

```
IFCLK toggle LOW then HIGH
while (have data):
        if (FF):
                SLWR = 1
        else:
                FIFO_DATAPORT_LOW = data(LSB)
                FIFO_DATAPORT_HIGH = data(MSB)
                SLWR = 0
                IFCLK toggle LOW then HIGH
                SLWR = 1
SKIP = 1
PKTEND = 0
IFCLK toggle LOW then HIGH
PKTEND = 1
```