SRI KRISHNA INSTITUTE OF TECHNOLOGY

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Department of Electronics Engineering-VLSI D&T

Subject Name: Low Power VLSI Design **Subject Code: BVL613A**

SEM: 6th

Faculty: Dr. N C Patil **Module-4 Unit Test** **Date: 04.05.26**

Note:Answer any five questions

SL No	Question	CO	Level	Marks
1	Explain the sources of power dissipation due to i) Input pattern dependence ii) Delay model in power estimation techniques	3	L2	5
2	Explain logic synthesis techniques for low power in four fronts and discuss power minimization in ASIC design flow at different abstract levels	3	L2	5
3	Explain power estimation techniques in VLSI design. Discuss their importance in low power design.	3	L2	5
4	Explain logic synthesis techniques for low power and discuss power minimization methods.	3	L3	5
5	Explain any two power minimization techniques in logic synthesis i) Precomputation Logic ii)State assignment, iii)Multilevel network Optimization, iv)Common sub expression Extraction,v)Path balancing, vi)Technology Decomposition vii) Technology Mapping., viii)Gate resizing	3	L2	5
6	Compare different circuit design styles for low power arithmetic components.	3	L3	5
7	With neat illustrations, Explain any two the following: (i)NORA full adder (ii) CVSL full adder. (iii)DCVSL (iv) CNTL (v) ECDL	3	L2	5
8	Discuss Probabilistic power estimation techniques i) OBDD ii) Markov Chain model	3	L2	5

Faculty Signature