Department of Electronics & Communication Engineering
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ASSIGNMENT – 5 (UNIT V)

CMOS Processing Technology

Descriptive Questions

1. (Long Answer)

Explain **Basic CMOS Technology**, **n-well process**, and **Twin-Tub process** with neat diagrams. Compare them.

2. (Long Answer)

Explain **Latch-up phenomenon** with parasitic SCR structure. Describe **internal and external latch-up prevention techniques**.

3. (Medium / Paragraph Question)

Explain **Interconnects, Vias, and Interlayer Dielectrics**. Why are RC delays important?

4. (Short Note)

Write a short note on Layout Design Rules.

5. (Short Note)

Write a short note on Process Enhancement Techniques.

MCQs (UNIT V)

1. Latch-up occurs due to activation of:
   a) PMOS
   b) Parasitic SCR ✔
   c) Resistor
   d) Capacitor
2. Twin-tub CMOS allows:
   a) No doping control
   b) Independent optimization of NMOS & PMOS ✔
   c) Only NMOS
   d) Only PMOS
3. Interconnect delay depends on:
   a) Resistance
   b) Capacitance
   c) Both ✔
   d) None
4. Guard rings help prevent:
   a) Noise
   b) Leakage
   c) Latch-up ✔
   d) Temperature rise
5. Layout design rules ensure:
   a) Functionality
   b) Manufacturability ✔
   c) More power
   d) Increasing leakage