

Activities Carried out during 2019-20 – II semester

Activities Conducted under the aegis of CoE in VLSI Design from Jan to April/May 2020:

1. Three-days follow-up session on "Advanced Digital Design using Verilog HDL" was conducted during **24-26 February, 2020** by Mr.Raja Bandi, Lucid VLSI.This focused on execution of mini projects.



2. A guest lecture in collaboration with IEEE CAS SB, GCET was delivered to II B.Tech (ECE) students on **15th February, 2020** by Dr. K. Vijay Kumar Gupta, CEO, LED Chip Indus Private Limited on the topic "**LED Chip Design, Fabrication and Applications**".





3. A guest lecture in collaboration with IEEE CAS SB, GCET was delivered to III B.Tech (ECE) students on **15th February, 2020** by Mr.. Avinash Yadlapati, Senior Director, Mirafra Technologies India Pvt. Ltd. on the topic "**CMOS Testing Methods**".



4. A two-week Student Development Program (SDP) in collaboration with IEEE CAS SB, GCET on "**VLSI Design using Verilog HDL**" is organized to II B.Tech students from 27th April to 7th May, 2020 by faculty members of CoE in VLSI Design.



Center of Excellence in VLSI Design
Department of ECE

in association with

IEEE CAS Student Branch Chapter
Geethanjali College of Engineering and Technology

presents

"SDP on VLSI Design using Verilog HDL"

Register at:
<https://bit.ly/SDP-CAS>



27th April, 2020 - 9th May, 2020