

CUKUROVA UNIVERSITY

ELECTRICS & ELECTRONICS ENGINEERING

2018-2019 SPRING TERM / EEE 424 SEMESTER PROJECT

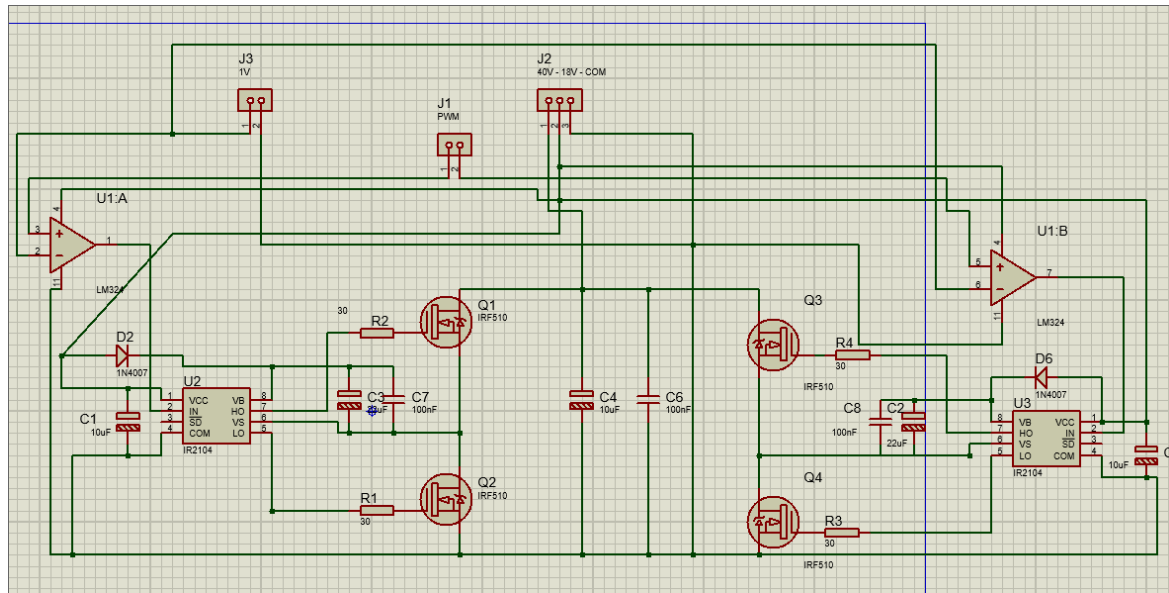
PROJECT TOPIC : Single Phase Full Bridge Inverter

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Used Equipments:

Materials	Description	Quantity
MicroController	MSP430G2553	1
Mosfet	IRF510	4
Mosfet driver	IR2111	2
Resistor	30 ohm / 8 Watt	4
Seramic Capasitor	100 nF	3
Electrolit Capasitor	10 uF	3
Electrolit Capasitor	22 uF (Bootstrap)	2
Diode	In4007 (Bootstrap)	2
Amplifier	LM324	1

1.SINGLE PHASE FULL BRIDGE INVERTER



In this project, the inverter is designed with spwm unipolar and bipolar methods. We designed an inverter in which we can get 100W - 150W output according to the materials we use.

Spwm bipolar and unipolar methods using MSP430 required pwm were produced. In order to adapt the single circuit design in 2 methods, 2 signals were generated from the MSP430. However, this problem was solved with the IR2111 integration since the MSP did not give dead time. IR2111 has about 650 ns dead time in its structure.

WHAT IS THE DEAD TIME ?

H and L switches from transmission to the cut or cut from the time before the transmission will start at the time and the driver's signals in the position to hold off the switch in the dead end is called dead time. The use of full bridge inverter design damages the circuit to be switched off at the same time or at the same time.

$$dT = \frac{Q}{I}$$

$$I = \frac{Q}{dT}$$

$$Q = Q_{gs} + Q_{gd} = 2.3 + 3.8 = 6.1 \text{ nC}$$

$$dT = t_r + t_{don} = 6.9 + 16 = 25.9 \text{ ns}$$

$$I = 6.1 \text{ nC} / 25.9 \text{ ns} = 0.2355 \text{ A is required at least.}$$

And the driver can supply 270mA at least when the Vcc is 10V . So it satisfies the current.

The gate drive resistor and bootstrap capacitor values affecting the speed of compaction were calculated using the formulas. In addition to the bootstrap capacitance, Parallel 100nF solid capacitor is used, the reason is to get the signal cleaner.

Gate Resistor

$$V_{LO} - I_G \times R_G - V_{GS} = 0.$$

$$R_G = (V_{LO} - V_{GS}) / I_G$$

$$V_{LO} \cong V_{CC} = 15$$

$$V_{GS} = 3V \text{ (Type.)}$$

$$I_G = 0.406 \text{ A}$$

$$\text{Therefore , } R_G = 29.556 \cong 30 \Omega$$

Bootstrap Capacitor

The minimum bootstrap capacitor value can be calculated from the following equation:

$$C \geq \frac{2 \left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{Ls} + \frac{I_{Cbs(leak)}}{f} \right]}{V_{cc} - V_f - V_{LS} - V_{Min}}$$

where:

Q_g = Gate charge of high-side FET

f = frequency of operation

$I_{Cbs(leak)}$ = bootstrap capacitor leakage current

$I_{qbs(max)}$ = Maximum V_{BS} quiescent current

V_{CC} = Logic section voltage source

V_f = Forward voltage drop across the bootstrap diode

V_{LS} = Voltage drop across the low-side FET or load

V_{Min} = Minimum voltage between V_B and V_S .

Q_{Ls} = level shift charge required per cycle (typically 5 nC for 500 V/600 V MGDs and 20 nC for 1200 V MGDs)

According to the datasheets,

$$C > 2.5\mu F$$

For this project we have chosen the bootstrap capacitor value 22 μ F.

In order to make the voltage coming from DC supply cleaner, parallel electrolyte and ceramic capacitor are added to dc supply.

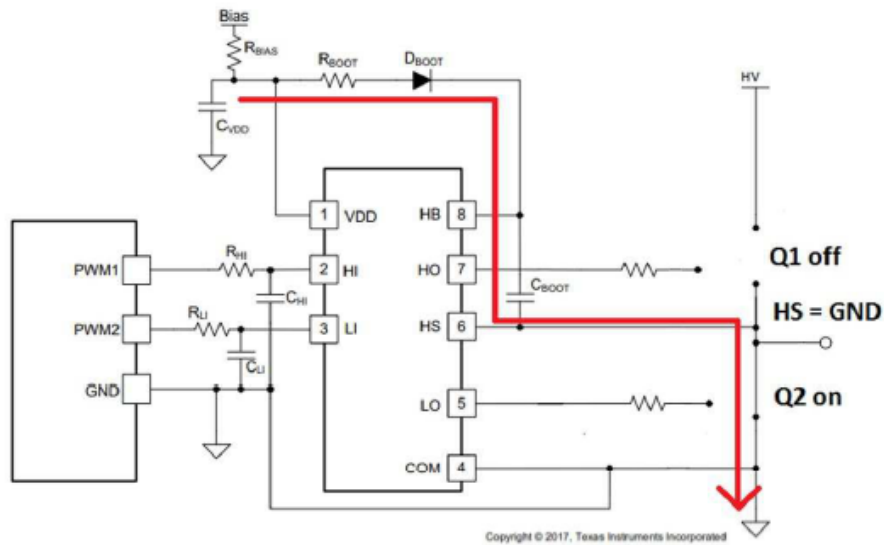


Figure 1. Bootstrap Charging Path

When the mosfet on the high side is off and the mosfet on the low side is on, the bootstrap capacitor is charging above the diode from Vcc.

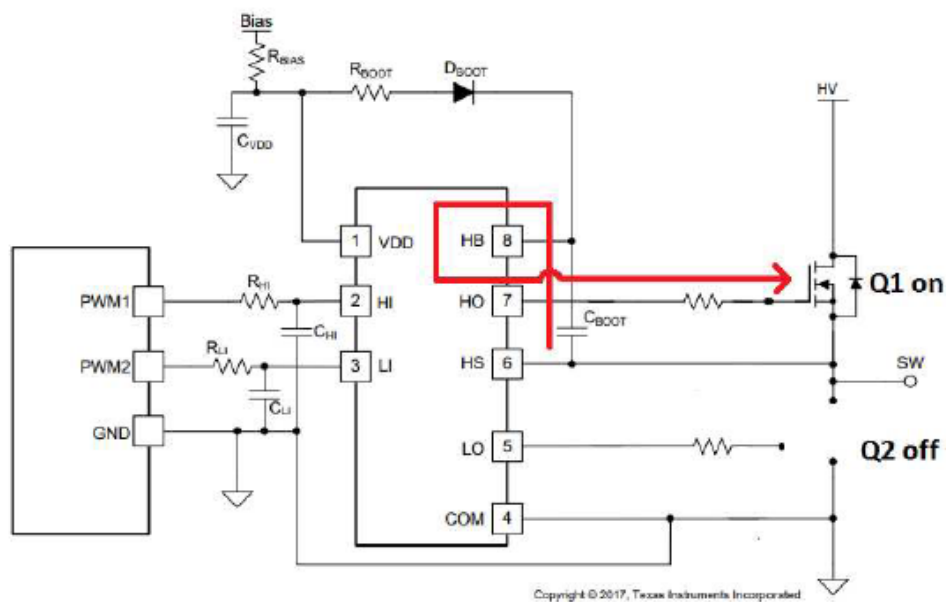
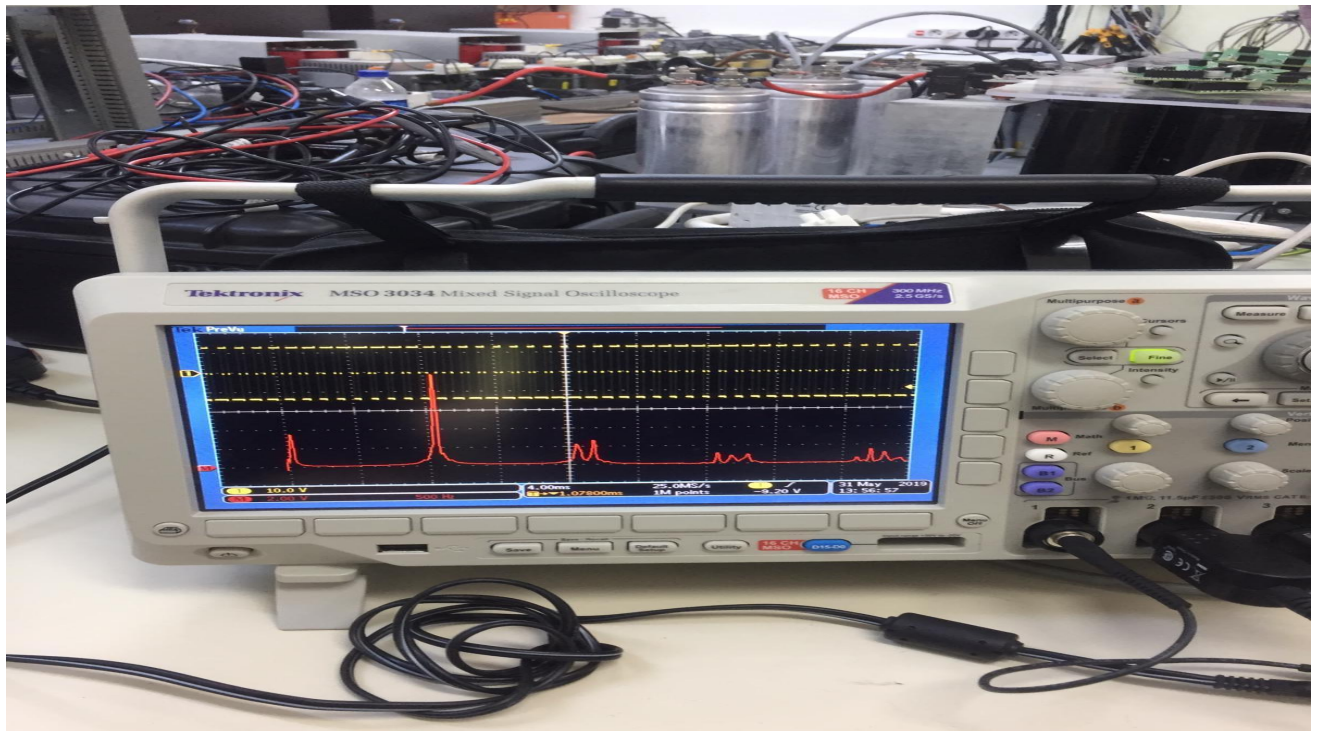


Figure 2. Bootstrap Capacitor Discharging Path

Conversely, the bootstrap capacitor that is charged will flow to high side mosfet above hs and hb pins. The Capacitor value is really important here. If selected too low, the energy will not be enough to drive the high side. If selected too high will reduce the switching speed. Therefore, the ideal value should be selected by experiment. Likewise, the gate resistance will affect the switching speed.

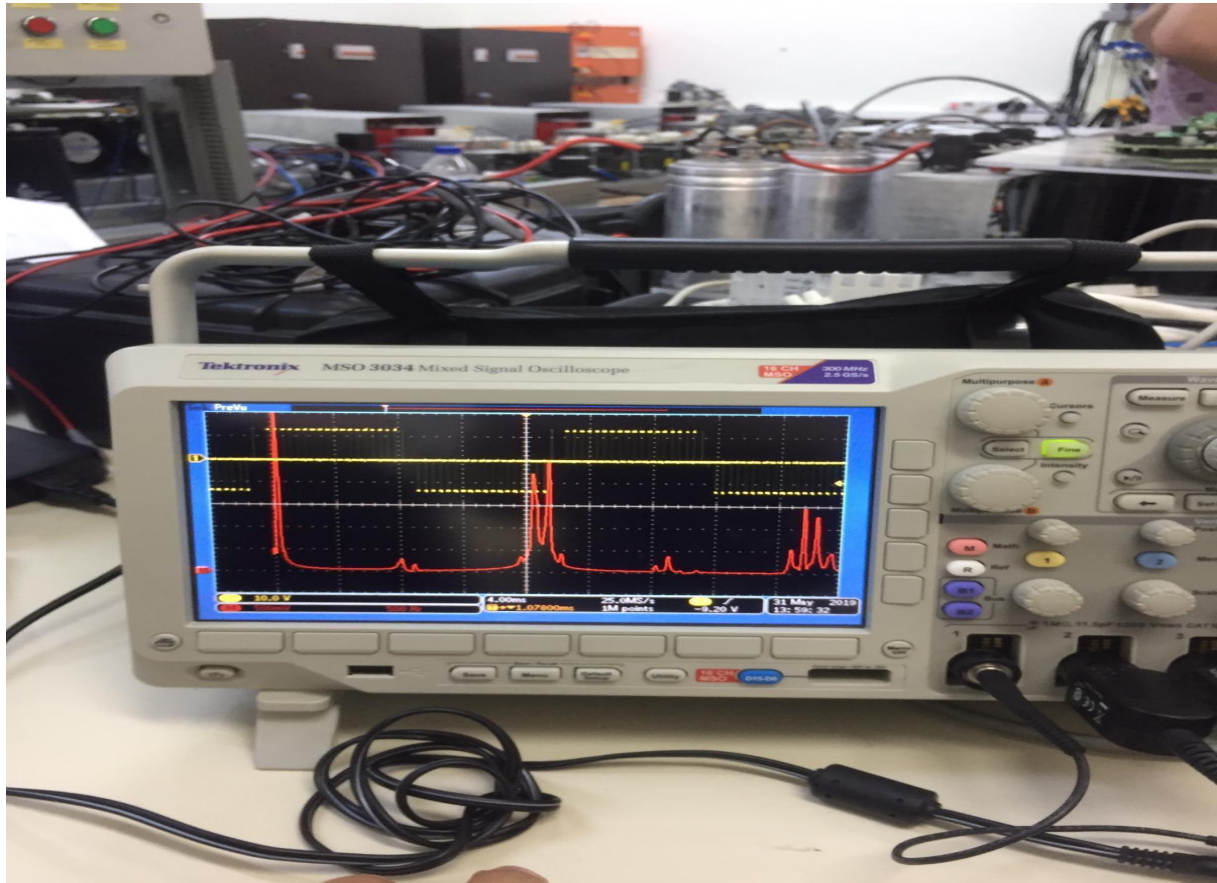
The IRF510 has a 100V VDS voltage and a 5.6 A Id current. So, approximately 50V should be given to these networks and the load should not be more than 3.3.5 a, otherwise the mosfets may burn.

2.Experiment results



Bipolar load signal

When we use bipolar technique, we see that the harmonics are only formed at the trigger frequency and the magnitude is equal to the supply voltage.



Unipolar Load Signal

When we use the unipolar technique, we observed that the harmonic is formed in double-layer frequencies and the size is lower than the bipolar technique.

3.CONCLUSION

Unipolar PWM:

1. Three voltage levels are there in the output
2. It requires two 180 degrees phase shifted sinewaves as modulating waves
3. It is complicated to implement
4. The harmonic performance is better
5. Filter requirement is less at the inverter output
6. Switching losses are less
7. Most extensively used
8. However, less suited for transformerless full bridge PV inverter

Bipolar PWM:

1. Only two voltage levels are there in the output
2. It requires only one sinewave
3. It is easier to implement
4. The harmonic performance is poor
5. Requires large filter at the output
6. Switching losses are more
7. Not much of use in the modern era.
8. However, better suited for transformerless full bridge PV inverter.