FAQs - please read before asking a question.

Google / Efabless / Skywater FAQs

9 Sep 2022

- Burak A
  - got design ready for MPW7
  - local precheck is working
  - Use PL_RESIZER_HOLD_SLACK_MARGIN to solve hold violations
- Ayan Ray
  - mixed signal
    - tool showing routing congestion over the analog
    - tool is crashing with this
    - Matt suggests check the obstructions are in the runs/<your run>/config.tcl
    - obstructions isn't working - looking for help on that
  - looking for any design using mixed signal design
    - https://gitlab.com/carllb52/mixed-signal-reram-mpw7-2
    - https://github.com/chrische-xx/mpw6
    - https://github.com/hpretl/iic-audiodac-v1
  - is there a way of doing interactive point to point routing.
    - the analog - digital routing is causing the problem
    - so just use openlane to place the macros, then route by hand.
  - opening an issue on openlane
- Burak A
  - precheck fail with metal4 >3m spacing to unrelated

6 Sep 2022

- What does CVC - circuit validity check
  - static checker, using spice level netlist
  - looking at interfaces,
  - propagates power & ground
  - compares voltages, diodes connections
  - send the error.gz

1 Sep 2022

- Vijayan Krishnan - what is the mpw-7a tag some of the features not working
  - Yes no problems. Just check that the tapeout job finishes.
- Matt recommends Submit early
- Hirosh Dabui - related to tinytapeout

- Aloke: Since MPW2 having problems. Best source for news:
    - #announcements channel
    - https://groups.google.com/g/skywater-pdk-announce
- Steven Bos sky130a vs sky130b
    - use sky130B
- Ashutosh Kumar
    - chipathon
    - running precheck precheck and getting xor errors
    - open the gds file precheck_results/07_JUN_2022___17_06_10/outputs/user_project_wrapper.xor.gds
    - if it doesn't work use the #precheck channel on the slack
- Lots of interest in https://tinytapeout.com

29 August 2022

- AHB interfaces? Matt suggests AXI also
    - https://github.com/shalan/Caravel_Chameleon_SoC.git this says it uses AHB in the description.
- What's the fastest ram to use?
    - Matt thinks openram

      OpenRAM characterisation with Andrew Zonenberg Part 3
- Next meeting will be Thursday 3pm CEST
-

7 June 2022

- Chithambara
    - use la_data_in to get signals from the riscv cpu
    - can use 128 at the same time
    - https://github.com/mattvenn/wrapped_instrumented_adder/blob/main/instrumented_adder_test/instrumented_adder.c
- Chithambara
    - gpio analog voltage. Confirm with Tim Edwards
- Chithambara
    - consistency check for analog projects
    - has to have a project instantiated in user project wrapper
- Ayan Ray
    - no simulation done in the precheck
    - analog pads can be swept

```
70
71      // Analog (direct connection to GPIO pad---use with caution)
72      // Note that analog I/O is not available on the 7 lowest-numbered
73      // GPIO pads, and so the analog_io indexing is offset from the
74      // GPIO indexing by 7 (also upper 2 GPIOs do not have analog_io).
75      inout [`MPRJ_IO_PADS-10:0] analog_io,
```

    - 76

- Anuj - make compress
    - can just compress the files in ./gds
- Anuj - precheck sometimes fail
    - only have a .gds or .gds.gz in ./gds
- Anju - how to submit for chip ignite shuttles
    - is there docs for chip ignite?
- Hanssel
    - question about timing reports
    - how to use SRAM
        - use the ones in the PDK
        - obstruction layer on top in the config.tcl
    - how to know if provider confirmed
- Aloc
    - how to do GL with sram: https://skywater-pdk.slack.com/archives/C016ULUQXDF/p1647537397267209
    - Matt suggests: replace your RTL with the GL and re-run simulations.
- Jure
    - how to do export compliance? go to activity
    - Harald Pretl has done it. Matt doesn't know how.
    - https://platform.efabless.com/projects/736
    - Does vexrisc have a debug port? Mat tdoesn't think so. use the LA or serial port.
- Tiago
    - how to do mixed signal
    - https://platform.efabless.com/projects/736
    - If your design is accepted: What does the board have?
    - WIP: https://github.com/efabless/caravel_board
- Hanssel
    - encryption accelerator. wants to run the software version to run in the vexrisc
    - is there an official way to add a library - not that Matt knows of.
- David/Mitch
    - With analog with more than 1.8v , use the HVL library instead of HD
    - can only see 6 bare pads.
    - Need LEF for analog circuits? if you need to route with digital, then you will need LEF, as that's what the router uses.
- Jure
    - the pcbs, how are they provided? populated, but only 3. then the rest of the 50 x WLCSP .

Questions to answer later

- confirm max input voltage for analog gpio
    - The maximum input voltage on the normal GPIOs is the value of VDDIO. The board that we provide will have this set to 3.3V, so that's the maximum voltage. However, the voltage regulator could be replaced, in which case VDDIO can be set as high as 5.5V.

- can gpio take negative ?
    - No. You cannot run a negative voltage to the GPIOs. The three reasons for bare analog pads on caravan are 1) Very high voltage, 2) Negative voltage, and 3) Very high speed. They are there to handle things that the GPIOs can't.
- with analog io can you go negative
    - yes the bare pads only
- can use analog ground as a negative voltage
    - No, for the same reason as above. Analog ground still has a reverse-biases ESD diode to global ESD ground (VSSIO), so negative voltages will forward-bias that ESD diode. (Technically, you can get to about -0.3V before anything bad happens, but that's generally not the intent of negative supplies for analog circuits.)
- Chithambara
    - in the 11 io analog pins on the top of the analog wrapper
    - 3 are used for io clamps
    - can those 3 pins be used as io or do they have to be dedicated as clamp
        - Yes. The clamps are not actually connected to anything, they just sit underneath the pads. Those pads can be used for I/O, just don't try to use them for noise-sensitive signals or fast signals, since they are capacitively coupled more strongly to the supply lines because of all the circuitry directly under the pad. Because the clamps are there, the pads are optimal for extra power supply connections, because you want your clamps as close to your supply input as you can get them. Also, the pads are bulked up with lots of extra metal so they can carry lots of current (if you need a number on that, I can look it up; I wrote it down in a spreadsheet somewhere).
- Anju - how to submit for chip ignite shuttles
    - is there docs for chip ignite?
- Hanssel - is timing constrained for hardening user project wrapper

```
2022-06-07T12:53:16.0138114Z report_checks -unconstrained
2022-06-07T12:53:16.0138419Z ============================================================================
2022-06-07T12:53:16.0155230Z Startpoint: wb_clk_i (input port clocked by user_clock2)
2022-06-07T12:53:16.0155666Z Endpoint: wrapped_instrumented_adder_kogge_6/wb_clk_i (internal pin)
2022-06-07T12:53:16.0156009Z Path Group: (none)
2022-06-07T12:53:16.0156256Z Path Type: max
2022-06-07T12:53:16.0156406Z
2022-06-07T12:53:16.0156549Z Fanout     Cap    Slew   Delay    Time   Description
2022-06-07T12:53:16.0157134Z ---------------------------------------------------------------------------
2022-06-07T12:53:16.0157528Z                          2.00    2.00 ^ input external delay
2022-06-07T12:53:16.0157877Z                   4.38   4.57    6.57 ^ wb_clk_i (in)
2022-06-07T12:53:16.0158166Z     11    1.08                        wb_clk_i (net)
2022-06-07T12:53:16.0158569Z                   7.42   0.00    6.57 ^ wrapped_instrumented_adder_kogge_6/wb_clk_i (wrapped_instrumented_adder_kogge)
2022-06-07T12:53:16.0158950Z                                  6.57   data arrival time
2022-06-07T12:53:16.0159435Z ---------------------------------------------------------------------------
2022-06-07T12:53:16.0159998Z (Path is unconstrained)
2022-06-07T12:53:16.0160166Z
2022-06-07T12:53:16.0160172Z
2022-06-07T12:53:16.0160179Z
```

- Vexrisc does have debug port? where is it documented?
    - yes - what was implemented is a debug UART that is connected directly the wishbone bus as a master. the uart port on the chip is muxed between the debug uart and the standard uart implement in the SoC. It is selected based on the debug_in input (high for debug uart) Here is a link to the testbench and the Lite code that implements this. The block diagram needs to be updated.
    - https://github.com/efabless/caravel_mgmt_soc_litex/tree/main/verilog/dv/tests-standalone/debug
    - https://github.com/efabless/caravel_mgmt_soc_litex/blob/aac1f07f993507d6369b31ae68ca5a5d3b242301/litex/caravel.py#L225 (edited)

31 May 2022

Questions that got answered

- Janani getting fails with the tests. can't see the outputs.
- Jure - running a sim - will come back
- Ayan - working on complete analog block.
    - can use logic analyser and wishbone at the same time? yes
    - precheck - what does it check? lots of stuff, Matt recommends running it all the time.
    - Matt recommends running tapeout asap too
- Chithambra
    - do we need to update the verilog, even if only doing an analog design?
    - Matt isn't sure - thinks its a good idea.
    - is there any detailed docs on analog projects?
    - Not really - analog-design channel on the slack is the best resource
- Dejan - should clone 6b or 6c? 6c.
- Dejan - are antenna violations important?
    - not really for shuttle runs - see this: https://www.zerotoasiccourse.com/terminology/antenna-report/
    - can sram instances be deep into hierarchy - no
        - https://github.com/mattvenn/zero_to_asic_MPW6
    - have you noticed precheck fails locally and succeeds remotely?
        - Matt hasn't but has seen it. suspects that it's docker images.
        - can you post about this in the #precheck channel
- Tiago - wants to implement a multiplier, async
    - what is a virtual clock?
    - Ayan: virtual clocks are used to model interface to the io pads.
    - but async multiplier within context of sync logic should be fine
    - good idea to test on fpga
- Ayan - how about GL sim:
    - Matt - https://github.com/mattvenn/gate_level_simulation
- Jure - rtl pass but gl fails.
    - trace is X (not Z)
    - check initial begin, and assumptions about registers being 0 at start.
- Janani - what is 1 bit gpio?
    - just for cpu core, can't control with user project
- Janani - should we do GL?
    - yes if possible
- Chithambara:
    - when try to install openlane. set openlane root folder, theres a problem with the install and the OPENLANE_ROOT
    -

Questions to answer next time

- check Janani's test bench.
- for analog projects is it necessary to have top level verilog.

24 May 2022

Questions that got answered

1. Tiago - what does io_out, io_in and io_oeb do.
    a. see gpio block diagram here: https://caravel-harness.readthedocs.io/en/latest/supplementary-figures.html
    b. https://www.zerotoasiccourse.com/post/understanding_caravel_gpio/
2. Tiago - how many shuttles will there be. At least 2 more, but hopefully more
    a. one of the metrics is how many applications are made
3. Tiago - digital vs analog designs. Matt links to the FAQ, recommends caravel unless you need > 50MHz bandwidth
4. Janani is going to be taping out on MPW6, 5 different designs with different configurations. Q1. What is the RTL test procedure for multi macros
    a. Use the same as the example tests
5. Janani had an error about the 'port vssd1 is not part of design', was because the module definition was missing the inout supply ports.
6. Janani wants to know about multiplexing multiple designs with lots of pins
    a. can use multiplex or tristate
    b. then use the logic analyser to choose which design is active
    c. can also use external inputs? yes no problem
    d. can use tristates with an assignment and the z assignment
7. Janani - what's the difference between gds generated by klayout vs magic
    a. klayout is considered experimental for now. use the one in results/final/gds
8. Aloke - for using srams, which is supported by openlane/ efabless
    a. 16bit 4kb
    b. srams generated by openram: https://openram.soe.ucsc.edu/
    c. instantiation example: https://github.com/mattvenn/zero_to_asic_mpw5/blob/6d54f2cf2d33c9d0b0ea0d5bba4269ed2c12f370/verilog/rtl/user_project_wrapper.v#L247
    d. can also use dffram
9. Ayan (ryan on slack) - voltage supplies
    a. https://caravel-harness.readthedocs.io/en/latest/supplementary-figures.html#power-domain-splits
    b. is there anything between the supply pins on the chip itself and the power rings around user_project_wrapper
10. Ayan - is there criteria on what designs are picked?
    a. no, it's random, but Tim Ansell has said earlier submissions will get some priority.
11. Ayan - is there any analog video that goes from beginning to end?
    a. join the #analog channel and ask for the best documentation on how to do it.

    b. Ask Harald Pretl, Stefan Schippers
12. Ayan - for mixed signal - is there concrete documentation for a mixed signal flow.
    a. This could be a good reference project: https://github.com/hpretl/iic-audiodac-v1
    b. This livestream with Thomas parry: https://www.youtube.com/watch?v=qABMStGDCTU
13. Janani
    a. don't see testbenches for the design. For Matt's zero to asic course submissions, I use my multi_project_tools that clones the designs and runs all the tests.
    b. https://github.com/mattvenn/wrapped_function_generator/blob/main/wrapper.v

Questions that didn't get answered

- Ayan: is there anything between the supply pins on the chip itself and the power rings around user_project_wrapper? (Tim Edwards) Physically, nothing substantial. In the layout, there is a metal resistor that virtually divides the net on the pin from the net in the core, so they have different names. And there is probably a few ohms' worth of resistance between the power pad and the user project, but it's mostly carried on wide metal5 buses, so it should not be significant (it's an improvement from MPW-one/MPW-two, which had a rather higher resistance into the user area supply ring).

21 Mar 2022

Questions that got answered today

1. Jorge Marin
    a. updated tools / tags / but had problems
    b. now want to try to submit mpw4
    c. doing analog
    d. matt will show how to use open galaxy to find the drcs
    e. video to show how to open xml marker database https://youtu.be/ieE24mvkLi4
2. Jure Vreca
    a. simple SoC with RISCV
    b. how to do pin assignments - use user_project_wrapper
    c. avoid first 8 and last 2
    d. if your design isn't tristate - set all oen_b to zero
3. Nanditha
    a. on 1 design shorts on vdda2 and vdds2 but not using those supplies
    b. other design mpw4 tools worked. did pass precheck. can submit - yes.
4. Ali Imran - @Ali Imran

    a. using sram macro provided on pdk file
    b. integrate sram - gives DRC violations, metal3 spacing is less than xxx
    c. give DRC errors when hardening, how does pre-check pass this.
    d. use obstructions to solve DRC: https://github.com/mattvenn/zero_to_asic_mpw5/blob/mpw5/openlane/user_project_wrapper/obstruction.tcl
    e. run precheck locally or on efabless platform , then should pass precheck
5. Gal -
    a. passes precheck - should he submit anyway - yes!
    b. simulations works
    c. GL doesn't work
        i. async design - maybe something gets optimised
        ii. Matt advises only to GL on design and not all of caravel to save time
        iii. bringout lots of debug signals to make debugging easier.
6. Tamas
    a. Caravel needs external flash
    b. for gpio defaults: gen_gpio_defaults.py - ask Tim Edwards on slack
7. Jorge Marin
    a. how to find the tag - look on the efabless platform
8. Jure Vreca
    a. date for submission
    b. not flexible :(
    c. have added sram macros
    d. process to add sram macros
        i. add macro name to macro.cfg: https://github.com/mattvenn/zero_to_asic_mpw5/blob/mpw5/openlane/user_project_wrapper/macro.cfg
        ii. add gds and lef to top level (not needed for sram though)
        iii. add instances to EXTRA_LEFS and EXTRA_GDS in config.tcl
        iv. need blackbox toplevel: VERILOG_FILES_BLACKBOX
        v. for srams, need obstructions on metal1 -> 4 to avoid DRCs
        vi. instance it inside user_project_wrapper.v
        vii. run make user_project_wrapper
        viii. hardening will fail with 2.5M DRC
        ix. only important thing is local and remote precheck
9. Jure Vreca
    a. in user project wrapper.v - is it ok to have logic in there.
        i. short answer is no
        ii. it is possible but it massively increases times for hardening and prechecks / tapeouts
        iii. here is an example: https://github.com/q3k/qf100
    b. better to put logic in a smaller block
        i. but make absolute floorplan 300x300 so it doesn't fall throught pdn
10. Jorge
    a. opened klayout & xml
    b. how to fix issues with analog. passed mpw4 precheck
        i. Jorge will post in #analog channel and tag Tim Edwards & Marwan
11. Tamas Hubai

    a. mpw5 tool goes wrong with congestion
    b. previously pass, but now get congested
    c. how to debug
    d. openroad gui: https://www.youtube.com/watch?v=5lkKp-gL1Ow
    e. Matt suggests try compare the config.tcl with all defaults against the mpw4 one.
12. How do we see what happened before:
    a. https://docs.google.com/document/d/1lKKtgcVXwYAe81afha8X3PpY4TEB0o6XIlWKrYT2A7c/edit

Questions that didn't get answered

1. Nanditha's repo regarding the shorts.
    a. fixed herself
2. Jorge
    a. opened klayout & xml
    b. how to fix issues with analog. passed mpw4 precheck
        i. Jorge will post in #analog channel and tag Tim Edwards & Marwan
        ii. see #analog channel
3. Tamas Hubai
    a. mpw5 tool goes wrong with congestion
    b. previously pass, but now get congested
    c. how to debug
    d. Matt has started a thread on this here: https://skywater-pdk.slack.com/archives/C016H8WJMBR/p1647880503102119
    e. we are looking for concrete examples of a design passing and failing with a tool change - if you can help please reply to the thread above.

18 Mar 2022

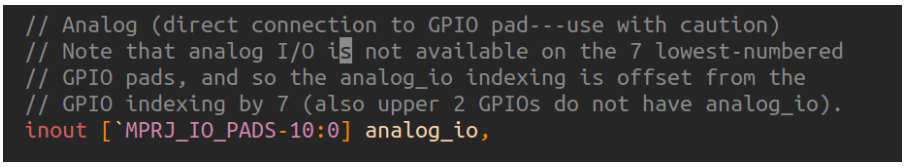
Questions that got answered today

1. get people's slack handles to reply to
2. Arman Avetisyan - asks about LI precheck: https://skywater-pdk.slack.com/archives/C01E06TUSC9/p1647617206313009
    a. matt suggested making the design smaller
    b. it's a template design so doesn't want to reduce it
    c. Efabless have a modified decap12 - try the alternative
    d. Jeff: when you rerun openlane, instruct openlane to use the new cell.

```
set ::env(DECAP_CELL) "\
       sky130_fd_sc_hd__decap_3 \
```

```
sky130_fd_sc_hd__decap_4 \
sky130_fd_sc_hd__decap_6 \
sky130_fd_sc_hd__decap_8 \
sky130_ef_sc_hd__decap_12"
```

3. Nanditha Rao asks - following previous procedure
    a. now we have a quickstart with make setup - Matt says use the new setup
    b. on previous version, could do make verify.
    c. now do: `make verify-io_ports-rtl`
4. Anuj Debey: wanting to use sram blocks
    a. https://www.youtube.com/watch?v=3-On3aQZCAc
    b. been tested up to around 40Mhz.
5. Connie Duong:
    a. followed github procedure
    b. gets email about stuff being broken. Yes, github actions are not working atm, so feel free to turn them off.
    c. Efabless are thinking of making it a template
    d. See whole flow on a video here: https://youtu.be/vJqP7ZR0Nrl
    e. docker sim-env is 10GB!
6. Anuj Dubey
    a. how do the chips get delivered, how to do bringup when the chip gets delivered to me
    b. has own cpu and own sram inside
    c. how to bring it up - how to program the sram from the VexRiscv cpu
    d. similar projects use a separate flash controller, with external flash on the board
    e. board from efabless: https://github.com/efabless/caravel_board/tree/main/hardware/caravel_pcb_v1
    f. also matt has shared sram access in zero to asic course submission: https://github.com/mattvenn/multi_project_tools/blob/main/docs/openram.md
7. Gal Nadrag
    a. GL simulation. Normal simulation works fine.
    b. GL has all X after 600us.
    c. The coulprit was the hex file. At 600us the spiflash had reached the end of the hex file and started loading undefined data. Adding extra 0s at the end of the file fixed the problem
    d. Jeff has seen this before, things weren't getting reset properly.
        i. have to find the point where X is and trace it back through the logic
        ii. and find the earliest point where it started
    e. SDF simulation - how to do it.
8. Nanditha: do all the designs that get to efabless --> and pass tapeout, get tapedout? Or are the designs selected based on some criteria?
    a. if we have more submissions than 40 - then we would have a selection process.
    b. google would choose
    c. sometimes Efabless have everything pass but then some issue comes up that means the project gets dropped. Generally people know if there's an issue.

    d. Efabless is working to improve the system to acknowledge submission process
    e. if you get your design taped out ready for MPW5 you are almost certain to get it made.
9. Dario Molina - doing analog
    a. caravel_user_project_analog - intended for high voltage or other advanced features: https://github.com/efabless/caravel_user_project_analog
        i. get bare pads with nothing. no esd. So good for high voltage / high frequency, but you need to do
    b. otherwise better to use caravel_user_project.
        i. 
```
// Analog (direct connection to GPIO pad---use with caution)
// Note that analog I/O is not available on the 7 lowest-numbered
// GPIO pads, and so the analog_io indexing is offset from the
// GPIO indexing by 7 (also upper 2 GPIOs do not have analog_io).
inout [`MPRJ_IO_PADS-10:0] analog_io,
```
    c. https://skywater-pdk.readthedocs.io/en/main/contents/libraries/sky130_fd_io/docs/user_guide.html
10. Anuj: Is the following approach correct:
    a. harden each module using standalone openlane setup,
    b. simply instantiate those modules as a macro in the user_project_wrapper.
11. Anuj: how to know what openlane image to use?
12. Armeleo Armosov: I am designing a GPIO + template that is placed inside caravan. Is there any ways that I could monetize my IP? Is there a way that efabless/sky130 can help me?
    a. Is there a way that efabless/sky130 can help me monetize it*?
    b. send an email to jeffdi@efabless.com
13. Janani: What's the difference between Caravel and Caravan?
    a. caravel_user_project and caravel_user_project_analog (standard vs bare/analog pads) - see question above.
14. Janani: Is there a limit on maximum number of designs that one can submit?
    a. no,
15. Darío: Efabless precheck says "You must create an Open MPW project to submit !" ?
    a. (Workspace on your MPW project - Select one - appears empty)
    b. probably you are missing the tags
    c. https://platform.efabless.com/open_shuttle_program/5
    d. if you get stuck then ask in precheck and shuttle channels
16. Anuj: How to best estimate the core_util? I just tried an example where I harden a picorv32a and then instantiate it with an SRAM. But it seems I ended up having insufficient DIE_AREA for input pins in this newly integrated design.
17. Olalekan Afuye:
    a. tapeout job fails after precheck passes
    b. post in precheck or shuttle channel and tag @jeffdi

Questions/ideas to answer during the week

1. setup simenv without docker as Connie as out of space
2. have an sram example setup with shared sram between caravel and user project

3. Dario - do we have a pad circuit or schematic or model that accurately represents the circuit that is implemented in each of the gpio pads. This would give enough information to know what to expect will happen. Wants to be sure for the future.
4.

11 Mar 2022

Questions answered today

1. Loading xml markers into klayout
    a. https://youtu.be/ieE24mvkLi4
2. Loading lef files to see defs properly
3. How to setup caravel to build
4. How to debug LVS errors Janani
    a. She will commit to github and post the link to the slack repo.
    b. #openlane channel
5. Mehdi - running checks fails on not finding GDS - not finding the gds
    a. Analogue project
6. Suggestion from Harald - use a flowchart
    a. Which gds / which file is inserted into what
7. Showing how to check a simulation, which are the most important traces
    a. Matt dropped vid link
8. Can ignore the management area root missing env var ? yes
9. How to get started with digital
10. Caravel clock speed
    a. It has a pll - calculator: https://github.com/kbeckmann/caravel-pll-calculator
11. What is user_project_wrapper vs user_proj_example
12. What is output enable pin do on the gpios?
    a. For tristate: https://www.zerotoasiccourse.com/post/understanding_caravel_gpio/

Questions to get answered during the week

1. Look at Janani's LVS mismatch - she will post.
    a. There were some nets disconnected in the wrapper
2. What is the filename required for an analog submission - Mehdi - https://github.com/msaligane/openfasoc_cryo
    a. answer: user project area gds was based on caravan and I was pushing it to the caravel one
3. Load on the wire to drive gpio. Because we don't know how much is the wire load from the macro to the GPIO.
    a. Nor the GPIO input. It may be a problem for very high speed signals.
    b. Tim Edwards: 3) Load on the wire---The signals from the user area `user_gpio_out` and `user_gpio_oeb` go to the gpio_control_block, where they

are driving a minimal digital gate load. FYI, I see that the same problem occurs in gpio_control_block as for the mgmt_protect: The inputs above should *not* be buffered in the gpio_control_block, for the same reason that they should be able to be left unconnected and not cause an issue with crowbar current.

   c. Tim Edwards: For `user_analog_io` , it's more of an issue because there is a lot of stuff hanging off that signal line, which goes directly to the pad, and that includes the bond wires, package pad, etc. I would assume maybe 2-5pF total load on that line, but it really depends on a lot of off-chip factors.

4. Gpio_defaults - what is it?
   a. Tim Edwards: The GPIO defaults is a way for the user to specify that the chip should start up with the GPIOs in a specific configuration. That allows the user to run their project independently of the management SoC. I had in mind the use case where the user has their own test board and just wants their project to power up and run without having to run a program on the management SoC. In that case, they will want their GPIO inputs and outputs set up appropriately. Also: Our way of mitigating the problem of not being able to load the GPIO configuration for any reason was to set all the GPIOs to user bidirectional. But the user may not be driving the OEB line and so the GPIOs may not be usable in that state. So it works best if the user just specifies which of their pins are inputs and outputs, and the chip will always power up configured properly for their project. Third reason: Some user projects start up immediately on power-up and have issues if the GPIO pins are not immediately available for use.
5. For analogue projects what to do with oeb pin (Matt guesses low for output , high for input).
   a. Tim Edwards: For analog projects where an analog signal is connected directly to the GPIO pad: The `user_gpio_out` and `user_gpio_oeb` pins are don't-cares, because the pad will be configured for analog use and all digital buffers will be completely shut down. (But note above: Because there's currently a buffer on these input pins in the design, as long as that's not fixed, the lines should be driven to either 0 or 1, although it doesn't matter which one).