

OPEN

Compute Project

Open Rack V3 48V PSU Specification

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• **Revision History**

Date	Version	Change By	Comments
08/24/2020	0.5	hamidk@	Added power system stability requirements on section 3.29 and appendix A. Added PMBus Spec, Appendix B. Added Modbus Spec, Appendix C. Added surge power requirements on Sec 3.28 Added power derating vs input voltage on section 3.1. Update fuse IR as 14kA on section 3.6. Updated section 3.12, 3.13, 3.15, 3.19, 3.20, 3.23, 3.27 Removed section 4.2 Output Voltage / Current Control Updated comms spec to support ModBus as well. Added section 3.30 PSU connector pinout.
8/26/2020	0.6	hamidk@	Updated Reset_H signal function on section 3.30. Updated inrush current as 30A on sec 3.7. Updated min PF as 0.95 on sec 3.9. Updated current sharing accuracy to be +/- 2% or better under load > 50% and +/- 5% or better under load >20%, sec 3.23. Added sec 4.2 Metering Accuracy. Added sec 4.7 Blackbox Function Added sec 3.29 Timing Requirements Added PLS (power loss siren) on sec 3.31
09/09/2020	0.7	hamidk@	Updated 3.27 Start-up Timing and synchronization Requirements Added block diagrams on sec 4 Updated sec 3.12 and 3.15, 3.23, 3.24, 3.25, 3.26, 9.1.1 Moved appendixes to attachments.
09/17/2020	0.75	hamidk@	Sec 3.27: 44V for 0.1 sec Sec 3.30: updated pinout Sec 4: added comms speed requirement and diagram.
9/21/2020	0.8	tjin@	Sec 7: Updated indicators and chassis interface.

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10/05/2020	0.81	hamidk@	Added facility i-t curve sec 3.6 Added rs485_addr2 on sec 3.30 (U1)
10/07/2020	0.82	hamidk@	Section 3.30: modified IShare to single ended. Added comments for internal pull-up and pull-down resistors for input signals.
02/08/2021	0.83	hamidk@	Updated sec 5.5 and 5.6 to clean up shock and vib req.
3/20/2021	0.84	benk@	Updated compliance section
4/26/2021	0.85	hamidk@	Removed CC operation Removed ITIC Updated, THD, droop, dynamic response, holdup time and BBU transition, Over power/current protection, current sharing, Forced discharge mode/ Peak power shaving mode, Pulse power requirements, Firmware Upgrade, and surge requirements.
7/6/2021	0.90	hamidk@	Modified 40ms rise time at full load, input overvoltage 345V for 50ms, 0.98 PF from 30% to 100% loads, accuracy requirements for 48V, 0.1uF cap for vo noise measurement, 10% min for dynamic response, 140% dynamic response requirement, Ishare full scale to 7V, increase Over power protection values, holdup time and BBU transition and pulse power width (design 2).
7/27/21	0.91	dmshapir@ jfern@ rvmerc@	Section 5.4: Reduced to single requirement for noise Section 5.5: Added required of PMI being inside shelf during test and testing to be done on soft & hard tooled parts Section 6: Rewording for thermal monitoring; updated value for back-pressure Section 7.1: Updated to new dimensions, new pictures Sections 7.2-7.9: Newly added sections Section 8.2: Added further MTBF requirements Section 8.4: Added mixed source requirement Added Section 8.6 - 8.11
8/18/2021	0.92	hamidk@	Added PMbus HW only and swap Modbus to PMbus by FW update requirement. Revised operation under 180V as disable by default. Removed sections: Last Power Failure Fault Conditions, Rectifier Failure Identification, Position
11/3/2021	0.93	rvmerc@	Updated Section 8.2 to revise requirements for Reliability Prediction/MTBF requirements Updated Section 8.7.2 to indicate ANSI standard for contamination requirement for the sheet metal/chassis

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01/06/2022	0.94	dmshap ir@	<p>Section 7.3: Updated clarification about materials</p> <p>Section 7.9: Updated mechanical drawings</p> <p>Section 8.7.2: Updated allowable material thickness and included Z18 minimum plating</p>
2/28/2022	0.95	hamidk @	<p>“Softly shut down” definition</p> <p>Fixed rise time to be fixed 60ms</p> <p>Updated Over Voltage Voltage Protection ranges</p> <p>Updated fuse interrupt rating to be at least 25kA</p> <p>Updated PF to be 0,9 for Vin>250V</p> <p>Updated iTHD for 10% load</p> <p>Updated 3V drop at 50% energy and related timings</p> <p>Updated OCP and SCP to 5s</p> <p>Updated Signal Ground coming from PMI – TOR to be isolated from the 48V power return through a 10 Ohm resistor</p> <p>Updated 3.28 Random timer values</p> <p>Included 3.29.2 48V to 51V Transition procedure</p> <p>Reduced pulse energy to 40%</p> <p>Added pin Y2 SYNC_STOP</p>
6/20/2022	0.96	hamidk @	<p>Sec 3.1: revised: If PSU input voltage and frequency goes out of the range while operating at any load value, PSU shall turn off its PFC and relay within 20ms and “softly shut down.”</p> <p>Sec 3.15: Note: For single step load from 10% to 100%, the output voltage shall not adjust from 51V to 48V.</p> <p>Sec 3.21: PSUs should sync using sync_start after shut down to power up together.</p> <p>Sec 3.23: Max setpoint increase (Capture range) for the current regulation is 500mV .</p> <p>Sec 3.28 and 3.29: increased delay time of DI_Sync_H stuck from 1s to 3s.</p> <p>Sec 3.32: pull up 100k for RS485_addr0 & RS485_addr1 & RS485_addr2. No pull up for BKP & PLS. Also, added Note: The pull up resistor of all the shared signals (PLS, BKP, RS485_ADDRx) should be individually in series with a Schottky diode, so the problem in one PSU doesn't impact other PSUs.</p> <p>Sec 4.1: PSU output voltage interruption due to FW upgrade shall be less than 5s.</p>

1. Scope

This document defines the technical specifications for Open Rack V3 rectifier used in the Open Compute Project.

2. Overview

This spec will define the single phase 48V power rectifiers that fits into the 48V power shelf. The rectifier is intended for use in a power shelf that is part of the rack, for supplying DC power to system loads. Several rectifiers with minimum of N+1 redundancy shall be included in the power shelf.

The rectifier operates based of “narrow-range 48V Architecture.” Based on this concept, rectifier output voltage is fixed at 51V and the regulated battery voltage is 48V. Benefits of this architecture compared to ORv2 with 40~60V dc voltage range are:

- Voltage range as low as possible to eliminate oversized voltage/current design
- Widely enable 4:1 fixed ratio converters and downstream conventional 12V PoL converters.
- Power to flow naturally, not with Software control and dependency.
- Enable simple fixed-voltage rectifier design.

3. Electrical Requirements

Requirements Brief Summary is given below:

- 3kW output power.
- Input rated voltage 200V to 277Vac with +/- 10%
- Output voltage 51V fixed on normal operation
- Peak efficiency> 97.5%, measured with fans
- Active power factor correction (meets EN/IEC 61000-3-2 and EN 60555-2 requirements)
- DC Output overvoltage and overcurrent protection
- AC Input overvoltage and undervoltage protection
- Over-temperature warning and protection
- Active current sharing on top of droop
- Hot insertion/removal (hot plug)
- Front to back air cooling
- Internally controlled variable-speed fan
- Ability to field FW upgrade (with bootloader)

“Softly shut down” definition: PSU reduce its voltage by 3V and wait for 6ms to give enough time for BBU to take over and then turn off output.

3.1 AC Input Voltage & Frequency

The rectifier shall be capable of supplying full rated output power over single phase input voltage range of 180 – 305V, and frequency of 47 – 63 Hz. Table 1 specifies the AC input voltage and frequency requirements for continuous operation.

Parameter	Typical	Min	Max	Power rating (W)
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AC Input Voltage	208, 230, 240Vac or 277Vac	180Vac	305Vac	Nominal Power
Frequency	60Hz	47Hz	63Hz	Nominal Power

Table 1 : AC Input Voltage & Frequency Requirements

Table above specifies the AC input voltage and frequency requirements for continuous operation. PSU minimum and max operating voltage can be limited further by software. If PSU input voltage and frequency goes out of the range while operating at any load value, PSU shall power off its PFC and relay within 20ms and “softly shut down.”

If enabled by software, the output power shall be derated linearly below 180VAC: 1.5kW at 100V and can “softly shut down” at 85V.

3.2 Start-up Sequence

The rectifier shall be able to start up under rated nominal power at the min AC input voltage (180 VAC) as specified in Table 1 above. With AC present, within specified parameters, the rectifier must always remain operational. The startup sequence shall be designed such that the rectifiers are able to meet the overall system start-up time and inrush current requirements specified later.

After AC voltage is applied, the internal bias supply starts, the microcontroller boots and keeps the PFC off as well as the dc-dc converter. Then the microcontroller closes the inrush relay and turns on all the converters.

3.3 Turn on - Cold Start

The output voltage of the rectifier shall be monotonic during turn on and turn off, there shall not have any reverse voltage during turn off.

- The dc output voltage rise time (10% to 90% of the output voltage) without external capacitors should be fixed 60ms (+/-10%) with 72A (120%) constant-current limit. If after 5s the output voltage isn't at the OK level, the PSU shall consider it as OCP and restart.
- The max capacitive loading on a single unit at power up is 10 mF.
- For any loads (from 'no-load' to 'max-load'), the output voltage will rise monotonically from 0V_{DC} to 51V_{DC}, without overshoot or ringing, at any turn on following application of AC input voltage, and anytime when the PSU resumes functionalities after an automatic protection condition (including parallel operations). The output voltage will fall monotonically from 51V_{DC} to 0V_{DC}, without undershoot or ringing, at any AC loss, and at any turn off caused by an automatic protection condition (including parallel operations).
- Output voltage shall never reverse polarity at the turn off (all conditions and converters).

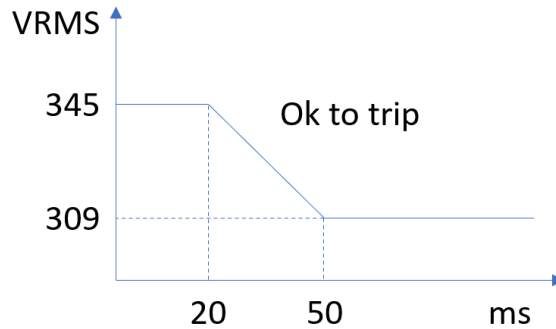
3.4 Turn on - AC Failure / Recovery

The rectifier shall recover automatically after an AC power failure. The start-up time requirement shall be same as that of a cold start specified in section above.

The PSU shall include a soft-start that promptly resets at any input AC loss > 20ms, or after any automatic protection conditions.

3.5 Input Over Voltage and Under Voltage Protection

The rectifier shall contain protection circuitry such that application of an input voltage below the minimum specified in Table 1 shall not cause any damage to the rectifier and “softly shuts down” while operating. The rectifier shall “softly shut down” if the input voltage is over 345V for 20ms or 309V for 50ms as shown in the graph below.



3.6 Input Over-Current Protection

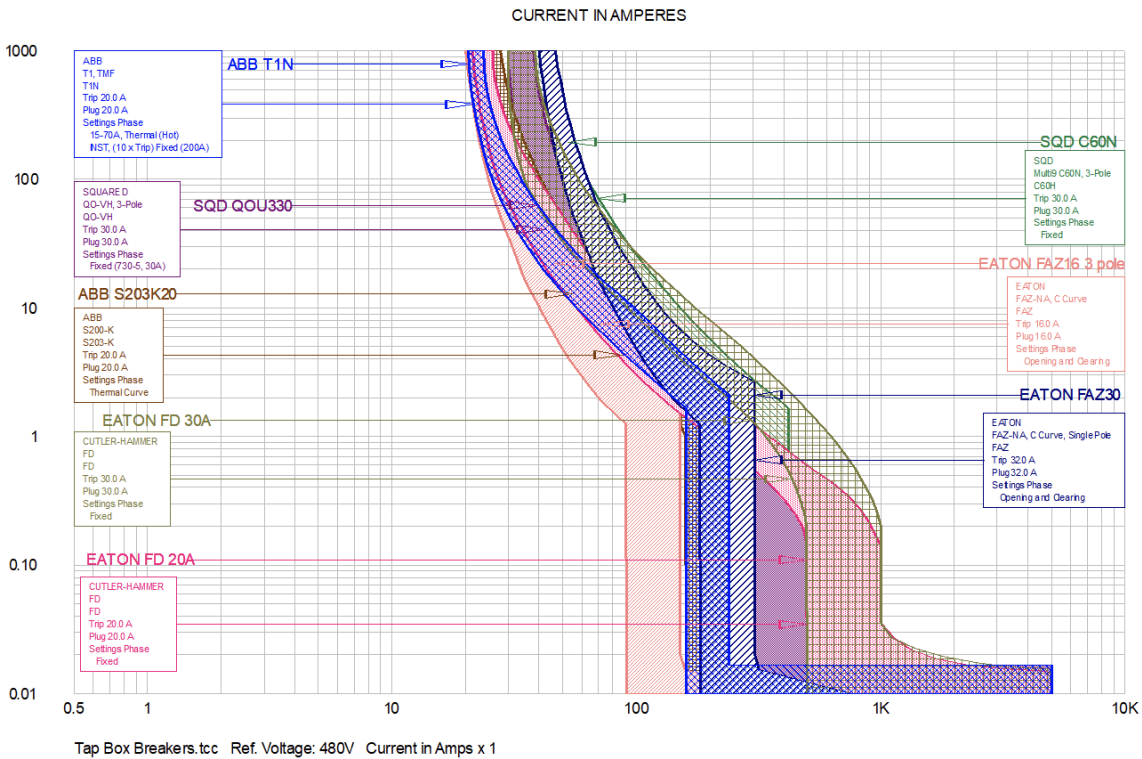
The rectifier shall incorporate primary fusing on *both phase and return lines* for input over-current protection to meet product safety requirements. Fuses shall be selected to prevent nuisance trips. Fuse may be internal to unit and need not be user serviceable. AC inrush current shall not cause the fuse to blow under any conditions. No rectifier operating condition shall cause the fuse to blow unless a component in the rectifier has failed. This includes DC output overload and short-circuit conditions. Fuse shall be approved by UL for an interrupt rating of at least 25kA.

PSU fuse shall be in coordination with Datacenter Tapbox breaker curve as given below.

NEC breakers are 20 and 30A (two ac feeds go to the power shelf – one PSU per input ac phase feed).

IEC breaker is normally 32A (one ac feed goes to the power shelf – two PSUs per input ac phase feed). (Ignore 16A breaker.)

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3.7 AC Inrush Current

Maximum AC inrush current from cold power-on shall be limited to no greater than 30A at any AC operating voltage and a temperature of 25C. This specified inrush current shall not include the X-Capacitors charging.

3.8 Efficiency

The efficiency of the rectifiers when measured at an AC input voltage of 208V~277V and with the cooling fans connected (with input and output voltage measured at corresponding connectors, at 25C ambient and after 30 minutes running at full load) shall meet the requirements outlined in Table below.

Load Range (%)	Peak Efficiency (%)	Min Efficiency (%)
30% to 100% of full load	> 97.5% @230, 240, 277V	> 96.5% @230, 240, 277V
	> 96.5% @208V	> 95.5% @208V

10% to 30% of full load	-	94% @208V~277V
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Table 2: Efficiency Requirements

3.9 Power Factor

The rectifier shall incorporate an active power factor correction circuit such that the power factor exceeds 0.98 from 30% to 100% loads. For loads less than 30% and down to 10% the power factor shall not be less than 0.95 for $V_{in} < 250V$ and 0.90 for $V_{in} > 250V$.

3.10 Total Harmonic Current Distortion (THD)

For input voltage of 208~277V:

Output load (% of max output load per module)	Maximum ITHD (%)
5-10	15
10-30	10
30-100	5

3.11 DC Output voltage

The DC output voltage of the rectifier shall be fixed at 51V @NL and 50.5V @FL while in normal operation. If commanded, the rectifier output voltage shall drop by 3V (48V @NL and 47.5V @FL). The rectifier shall supply rated power for the entire range of DC output voltage of 47.5V to 51V.

3.12 DC Output set point voltage accuracy

The rectifier set point output voltage accuracy at 100% load shall be +/- 0.25% or +/- 0.125V for both 51V and 48V. This can be accomplished by EoL calibration.

3.13 DC Output droop voltage

The rectifier droop voltage (0%-100%) shall be 0.5V by default (with the tolerance of +/- 0.125V). That means output voltage is 50.5V at 100% load and 51V at no-load. The droop extends linearly to 150% (it means at 150%, the droop is 0.75V, and voltage is 50.25V).

3.14 DC Output Voltage Ripple & Noise

The DC output voltage ripple and noise shall not exceed 500 mV peak to peak. Ripple and noise are defined as periodic or random signals over a frequency band of 5Hz to 20MHz measured across a steady-state resistive load. Measurements shall be made differentially using an oscilloscope with 20MHz bandwidth limit enabled. Compliance will be verified using a 0.1uF capacitor connected locally to the oscilloscope probe tips during this measurement.

3.15 Dynamic Response

Under these testing conditions, the DC output voltage shall not vary by more than specified for undershoot and overshoot with 3mS settling time (with and without capacitive loading on a single unit of 10 mF). The measurement shall be from the new steady state value (due to droop) to the voltage spike/dip peaks during a transient load.

step load increase or decrease	Frequency	Transient load rate	Max undershoot and overshoot
50% step load (10% min. load)	20 Hz	1 A/uSec	0.5V
90% step load (10% min. load)	20 Hz	1 A/uSec	1V
140% step load (10% min. load)	20 Hz	1 A/uSec	1.5V

Note: For single step load from 10% to 100%, the output voltage shall not adjust from 51V to 48V.

3.16 Overshoot at Turn on / Turn off

The output voltage overshoot upon the application or removal of AC input voltage, under the specified input voltage defined before, shall not exceed 1V.

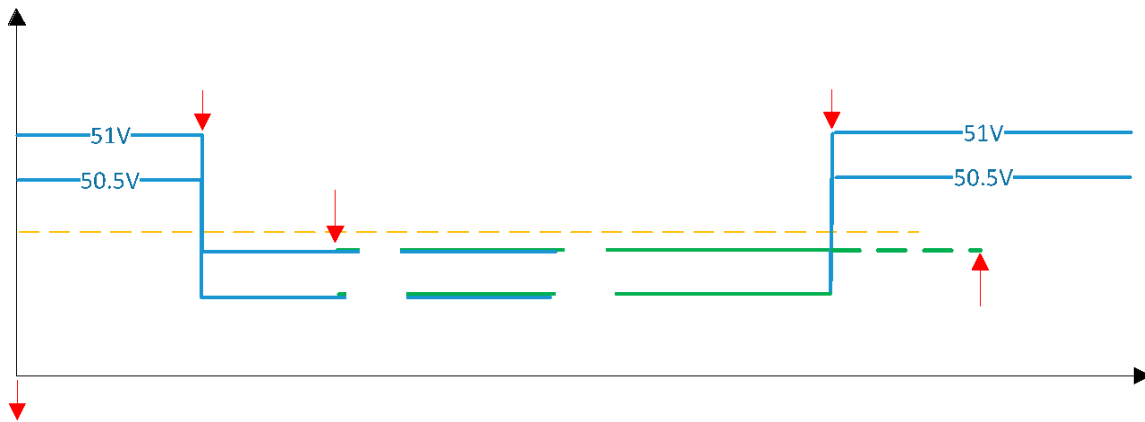
3.17 Hold-up Time

Holdup time requirements at different load power are given in the table below. Holdup time is calculated from the time ac input is lost till the time the output voltage is out of acceptable 48V range.

load power	holdup time (ms)	Energy (J)
100%	20.00	60.0
110%	18.18	60.0
120%	16.67	60.0
130%	15.38	60.0
140%	14.29	60.0
150%	13.33	60.0

3.18 PSU-BBU transition

Graph below shows the PSU requirement to transition to BBU in case of ac outage. PSU voltage should drop by 3V after its holdup energy is lost by 50% or 30J.



Per the scheme above, for the worst case that ac outage and pulse power happens at the same time (and pulse power remains constantly), PSU shall transition to BBU seamlessly as calculated on the table below.

load power	holdup time (ms)	time before 3V drop (ms)	remaining time after 3V drop (ms)
100%	20.00	10.0	9.0
110%	18.18	9.1	8.1
120%	16.67	8.3	7.3
130%	15.38	7.7	6.7
140%	14.29	7.1	6.1
150%	13.33	6.7	5.7

3.19 Output Over Voltage Protection (OVP)

The rectifier shall shut down for DC output voltage exceeding 52.5V and the reacting time shall not exceed 200ms. For DC output voltage shall never exceed 54V (fast OVP).

3.20 Over power/current protection

If a PSU is overloaded higher than the values listed below in sections 3.20.1 and 3.20.2, it shall “softly shut down”, meaning reduce its voltage by 3V and wait for 6ms to give enough time for BBU to take over and then turn off output. If PSU is still overloaded, it shall shut down. After an overload shut down or in case of 3V drop if there is no overload, PSUs shall retry to sync together and turn on once every 5s.

3.20.1 Over power/current protection limits

- Average power more than 3.3kW for 10s.
- Average power more than 3.6kW for 100ms.
- Repetitive pulse power more than the pulse power envelope specified (up to 150% load).

3.20.2 Constant Current Protection

Constant Current mode shall be triggered at 155% load. Output reduce voltage by 3V if any of the conditions below are met:

- Constant current mode dwell for 10msec
- Output droops <48.5V due to constant current mode.

3.21 Output Short-circuit Protection

The rectifier shall employ short-circuit protection to protect the rectifier and attached load in the case of an output short-circuit or other output overload condition.

If the rectifier voltage is lower than 10V (short circuit condition), the rectifier shuts off immediately. No component shall damage. The protection shall be implemented with a hiccup mode. it tries to restart 5 times every 5 seconds and then locks out. PSUs should sync using sync_start after shut down to power up together.

3.22 Over Temperature Protection

The rectifier shall employ over temperature protection for both ambient over temperature and internal thermal temperature to protect the rectifier. The rectifier shall “softly shut down” under over temperature condition and recover after certain period after the over temperature condition is removed.

The OTP circuit shall incorporate built in hysteresis such that the power supply does not oscillate on and off due to temperature recovering condition. The OTP event shall be reported as a fault condition.

3.23 Active Current Sharing Accuracy through analog bus

The rectifiers shall have a dedicated analog bus with slow bandwidth for active current sharing. With the maximum number of rectifiers connected in the system, the current sharing accuracy shall be +/- 2% or better under load > 50% and +/- 5% or better under load >20%.

Max setpoint increase (Capture range) for the current regulation is 500mV.

The PSU input impedance of the current sharing shall be 30kR & 100pF or better.

Current sharing bus (Ishare) full scale voltage shall be 7V and scale up linearly up to 150% (10.5V). BW of Ishare shall be 50Hz.

In the event of Active current sharing gets broken, the PSU shall share the load through voltage drooping with accuracy up to 5 times the values above. The failure of a module inside the PSU should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and be able to hot-swap.

3.24 Rectifier physical addressing

Four rectifier signal pins are used for physical addressing. There are digital signals that should have internal pull up resistors inside the rectifier. On the power shelf, these pins can be grounded (0) or left open (1) to determine rectifier location as below:

Rectifier location 1-1 (row-column): 0000

Rectifier location 1-2: 0001

Rectifier location 1-3: 0010

.

Rectifier location 2-1: 0110

.

and so on.

3.25 48V/51V output voltage selection

Rectifier output voltage is nominally 51V (droop range 50.5-51V). When commanded by SW, rectifiers shall change their output voltage to 48V (droop range 47.5-48V). Default output voltage is 51V.

3.25.1 Forced discharge mode/ Peak power shaving mode

This feature can be used for datacenter peak power shaving.

Starting procedures:

- Rack Monitor sends Modbus forced discharge commands to PSU and BBU including forced discharge time.
- BBUs start and increase output voltage to 51V-50.5V (0.5V droop from 0% to 100% load).
- PSUs reduce output voltage to 48V.

Exiting procedures:

The forced discharge will end in the following scenarios: 1) Forced discharge time register expired; 2) Rack monitor disabled forced discharge; 3) BBU remaining capacity falls below 120s(TBD)

In Scenarios 1-2,

PSUs raise voltage back to normal range 51V-50.5V

BBUs exit from discharge mode and enters standby/charge mode

In Scenario3,

BBUs exit discharge mode when remaining capacity is below 120s(TBD).

PSUs detect bus voltage <50V for >10s then raise voltage back to normal.

Sync_start shall be used for BBUs entering and exiting from forced discharge mode.

3.26 LED

The PSU will have a single blue and single amber LED mounted near the PSU handle for accessibility. Following are power supply LED States:

LED 1, Blue LED:

- 1) **Blinking Blue @ 4Hz frequency:** Sync Start State, PSU is ready to turn on its output and awaiting the sync Start signal
- 2) **Solid Blue:** 51V is ON and available
- 3) **No LED:** 51V output off

LED 2, Amber LED:

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- 1) **Blinking Amber @ 4Hz frequency:** Bootloading
- 2) **Solid Amber:** Primary/Secondary/Fan/bootloading Failure and/or loss of DC output
 - (refer to PSU Modbus/PMbus registers for specific failures)
- 3) **No LED:** fault NOT present/condition 1 and 2 are false.

- NOTE: toggling AC input power will reset the solid/blinking yellow fault light but will come up again if faults re-occur.
- Only one of the 3 conditions per LED will be applied at ALL time.

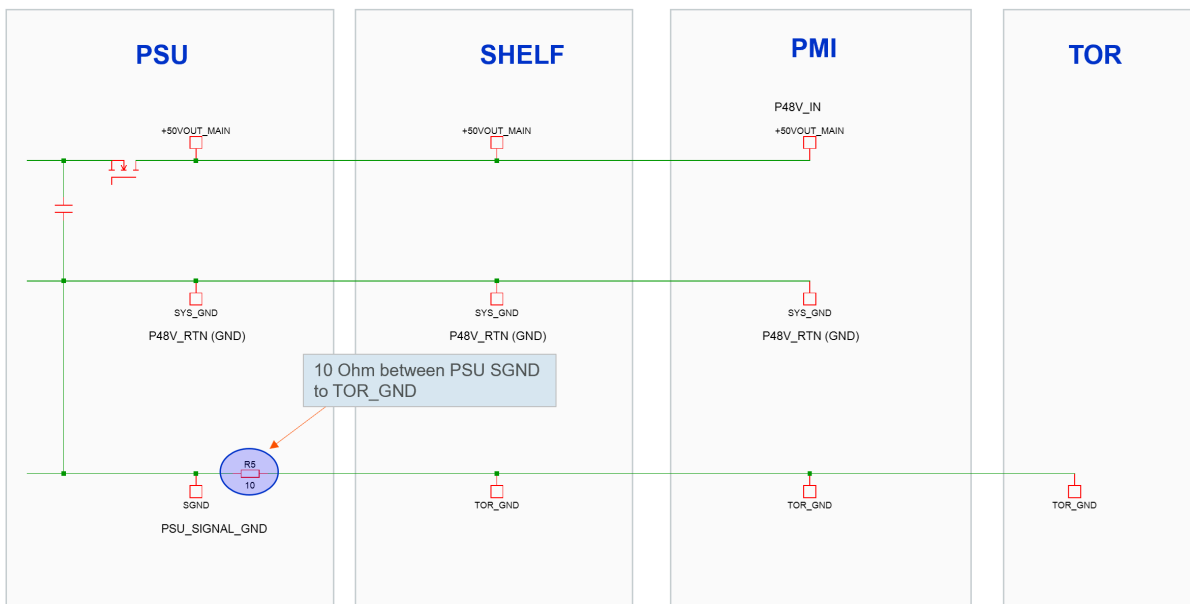
Refer to the mechanical drawing for the suggested location of the LEDs.

3.27 Grounding

The protective earth ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

Power supply output voltage return *shall not* be connected to Ground.

Signal Ground coming from PMI – TOR shall be isolated from the 48V power return through a 10 Ohm resistor to avoid ground loop between TOR and PSU, see below.



3.28 Random timer

Under any conditions of dissipative load, capacitive load, temperature, with or without backup voltage connected to the PSU:

- Max time for PSU to be “power-up ready” after AC voltage starts is 2.3s.
- After “power-up ready”:
 - When there is no dc voltage on the bus (first AC turn on) the power shelf shall be randomized with 0~2 second window to give each power shelf a random turn-on time (six PSU turn-on is synchronized).

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- When there is dc voltage on the bus higher than 44V for 0.1 sec (BBU is discharging), the power shelf shall be randomized with 0~5.7 second window to give each power shelf a random turn-on time (six PSU turn-on is synchronized).
- The power shelf shall turn on with only 1 PSU inserted into any slot.

Note: The random numbers above shall be dynamically generated immediately after each AC recycle, and not generated one time and then stored in the EEPROM for future usages.

Item	Description	Min	Max	Units
T_power-up_ready	Time for PSU to be power-up ready	1	2.5	seconds
T_random_noBBU	0-2 second initial turn on random delay without BBU discharging	0	2	seconds
TON_noBBU	Time 51V _{DC} turns on after shelf receives AC input without BBU discharging.	1	4.5	seconds
T_random_BBU	0-5.5 second turn on random delay after BBU discharging	0	5.5	seconds
TON_BBU	Time 51V _{DC} turns on after shelf receives AC input with BBU discharging.	1	8	seconds
TSYNC	After all PSUs in the shelf are ready to start till when 51V _{DC} will start	2	5	msec
T-Max_ON_noBBU	Max PSU turn-on time without BBU in case of sync failure	6	7.5	seconds
T-Max_ON_BBU	Max PSU turn-on time with BBU in case of sync failure	9.5	11.0	seconds

3.29 Transition and synchronization Requirements

3.29.1 Start-up (0V to 51V) Transition procedure

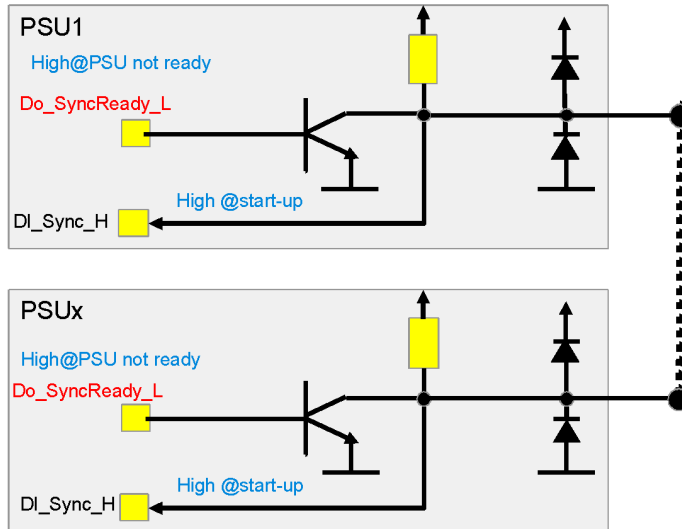
Each PSU has a small circuit as shown below and the circuit output (called SYNC_START) of all PSUs are connected together on the power shelf backplane.

- 1) Each PSU sets its uC Digital output signal (Do_SyncReady_L) to low when the PSU is ready to turn on the output.
- 2) Only PSU in SLOT #1 generates random timer and set Do_SyncReady_L to low when ready and random timer is finished.
- 3) The PSUs will turn on the output when the uC Digital input sync signal (DI_Sync_H) is high.
- 4) If DI_Sync_H kept stuck low for 3s more than the max random timer limit (which is 2s without BBU and 5.5s with BBU), the PSU shall turn on immediately.

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- 5) if PSU1 is not installed or its Do_SyncReady_L stuck low, the other PSUs shall turn on when the DI_Sync_H is high. In this case random timer doesn't exist.

Please refer to section 3.3 for the timing and constant current value requirements during the clod startup.

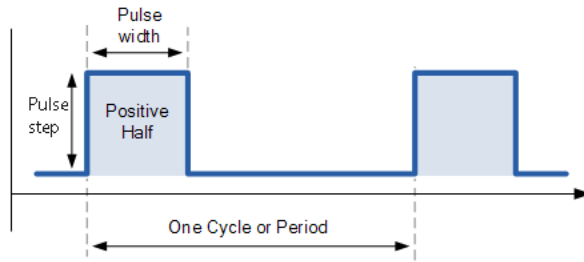


3.29.2 48V to 51V Transition procedure

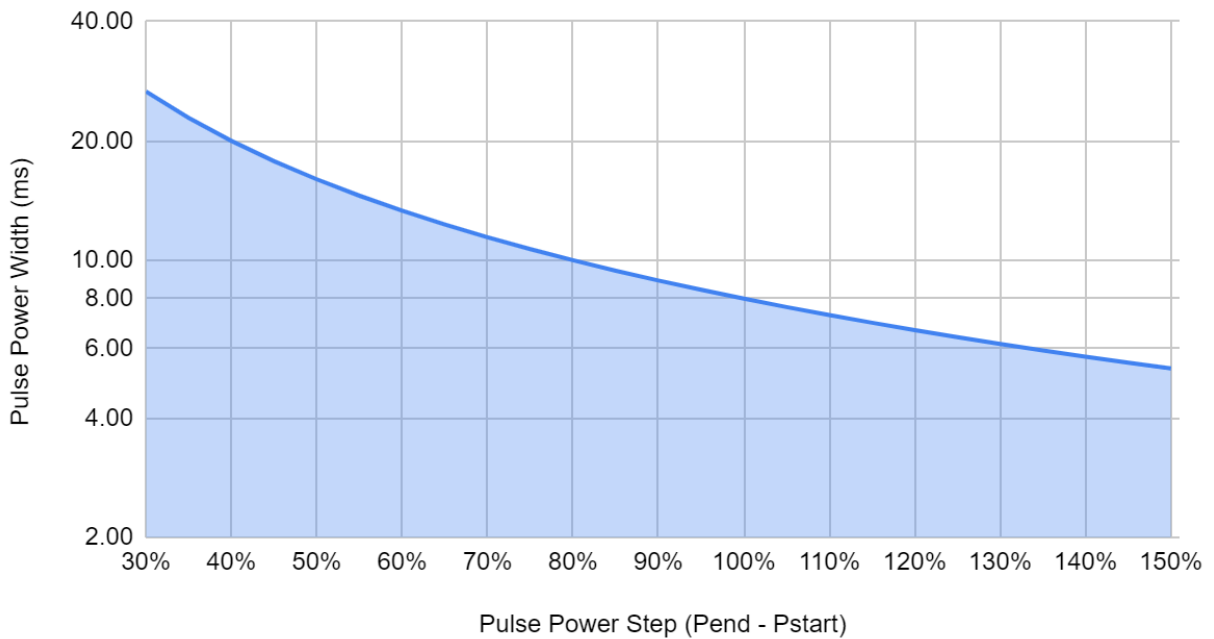
The same SYNC_START circuit as shown above is used here.

- 1) When PSU enters 48V output mode, it sets "Do_SyncReady_L" signal to HIGH.
- 2) If there is no over power or over current condition for 5s, each PSU sets "Do_SyncReady_L" signal to LOW.
- 3) If signal "DI_Sync_H" is HIGH (HIGH when all PSUs in parallel ready to adjust), then change constant current level to 120% and adjust output from 48V to 51V.
- 4) If the signal "DI_Sync_H" is stuck LOW for 5s, the PSU shall adjust its output from 48V to 51V.
- 5) If the PSU output did not reach 51V in 5s, then it return to 48V mode, set constant current level to 155%, and go to step 1).

Refer to diagram below that covers both 48V to 51V and 51V to 48V transitions.

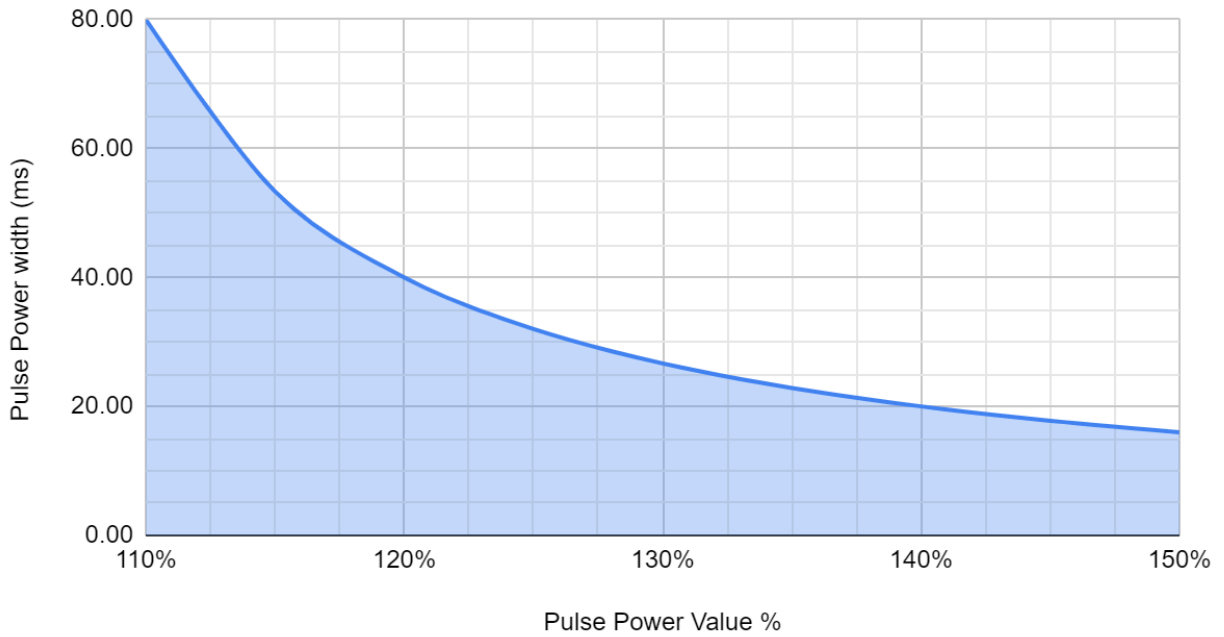


Allowable peak power step



In order to meet the Pulse power requirements as the graph above, the dc-dc converter should meet the following absolute pulse power requirement as shown below. This graph comes from the worst case of Pstart as 100%.

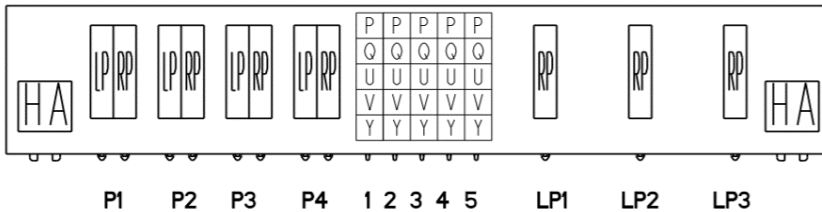
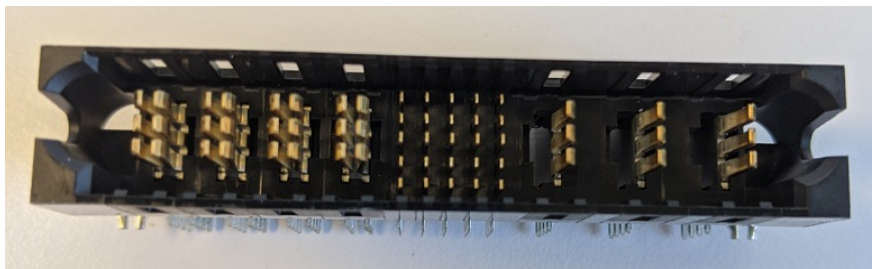
dc-dc converter pulse power requirement



3.31 Power system stability requirements

Please see appendix A for power system stability requirements.

3.32 PSU connector pinout



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P1 & P2	48V positive
P3 & P4	48V return
LP1	Earth
LP2	ac phase
LP3	ac phase

Note: P3, P4, and LP1 mate first. U3 is short pin.

PSU Pinout	Signal Name	Type	Bus	Function	Comments
P1	PSU_A0	Input		Address 0 - PSU ID A0	Internal pull up 10k to 3.3V
P2	PSU_A1	Input		Address 1 - PSU ID A1	Internal pull up 10k to 3.3V
P3	PSU_A2	Input		Address 2 - PSU ID A2	Internal pull up 10k to 3.3V
P4	PSU_A3	Input		Address 3 - PSU ID A3	Internal pull up 10k to 3.3V
P5					
Q1	Ground	Ground			
Q2	Alert	Output/Active Low	individual	Logic "Low"= Fault or Warning Logic "High"= OK	Internal pull up 10k to 3.3V PSU Alert
Q3	Reset_Latch_Fault	Input/Active high	individual	high for 1-2s = clear faults and start PSU if not operating due to a fault	Should be enabled by SW. Internal pull down 10k resistor.
Q4	RS485_addr0	Input	Share bus		Internal pull up 100k to 3.3V
Q5	RS485_addr1	Input	Share bus		Internal pull up 100k to 3.3V
U1	RS485_addr2	Input	Share bus		Internal pull up 100k to 3.3V

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U2	BKP	Output/ Active Low	Share bus		No pull up or pull down, Open collector output. All PSUs Ored together.
U3	PSKILL (Short Pin)	Input/ Active High		Logic "Low"= Output Turn on Logic "High"= Output Turn off	Quick shut down Output, mitigate hot unplug arcing. Internal pull up 10k to 3.3V.
U4	RS485A	BI	Share bus		
U5	RS485B	BI	Share bus		
V1	Ground	Ground			
V2	I2C_SDA	BI	share bus	I2C Data	
V3	I2C_SCL	BI	share bus	I2C Clock	
V4	Ground	Ground	share bus	I2C ground	
V5	PLS (power loss siren)	Output/ Active low	share bus	Logic "Low"= Input is not OK for 45Sec Logic "High"= Input is OK	No pull up or pull down, Open collector output. All PSUs Ored together.
Y1	ISHARE	Analog	share bus	Main Output current share bus	
Y2	SYNC_STOP	BI	share bus	Synchronizing turn-off main output (no use case currently)	Internal pull up 10k to 3.3V
Y3	SYNC_START	BI	share bus	Synchronizing turn-on main output	Internal pull up 10k to 3.3V
Y4	VOUT_SEL	Input	share bus	Logic "Low"= Set Output 48V Logic "High"= Set Output 51V	Internal pull up 10k to 3.3V, Default Output is 51V.
Y5	Ground	Ground			

Note: The pull up resistor of all the shared signals (PLS, BKP, RS485_ADDRx) should be individually in series with a Schottky diode, so the problem in one PSU doesn't impact other PSUs.

4. Communication

The rectifiers shall be able to communicate on PMBus (up to 100kbps) and ModBus (up to 115kbps). See related Appendices.

At default, Modbus is active and PMBus is hardware only. The design should allow to switch to PMbus communication with a FW update.

The software interface shall be operational when the AC is present or when the DC output bus is powered up by other power sources. Refer to the register maps for fault/read/write registers that PSU should communicate.

4.1 Firmware Upgrade

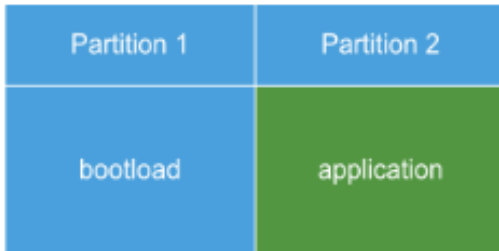
The interface shall allow the user to re-flash firmware on the device. Firmware upgrade shall result in no power interruption on the shelf level (the unit being upgrade can go offline.) Upgrades can be done 1 rectifier at a time. PSU output voltage interruption due to FW upgrade shall be less than 5s.

The PSU FW shall maintain regulation on the output during Send, Install and verification of the new FW, and only require a soft reset (that may reset the output for a short period in a few seconds)

Suggested implementation

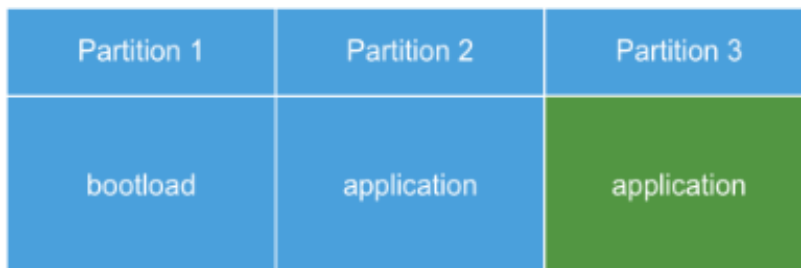
Traditional designs have the following implementation on it is micro flash at high level:

Upon micro boot, when fw update is not enabled, ie. the unit is not being updated, the unit boots into the application mode and carries out the operation



As an update is initiated, the bootloder partition is leveraged for the duration of the update, the new FW is then installed in the application partition, a soft reset occurs, and unit boots into the newly installed application

In the improved method, the micro flash can be split in 3 partitions.



The application operations can carry as before. so will the FW update, however, the update will occur on the partition that is not currently running, once the FW install is complete, the unit resets and boots into the newly installed image. This has the benefit of having a last good copy of the FW on the PSU as all times as well.

Note that this implementation depends on the architecture of the microcontroller used, in some cases, 3 separate partition is not required, and a similar process can take place with two partitions in the flash and the presence of a ROM.

4.2 Metering Accuracy

Accurate reporting of input power (power factor, input current, input current harmonics and voltage) and output power (output current and voltage) readings shall be reported via communication system at all rated voltage.

The accuracy shall be maintained across the operating temperature range and between 200Vac and 305Vac.

parameter	Load	Accuracy
AC input power	<10%	±25W
	10-20%	± 5%
	20-100%	±3%
AC input current	<10%	±0.5A
	10-20%	±2%
	20-100%	±1%
AC input current THD (Error difference not %)	<10%	±10%
	10-20%	±2%
	20-100%	±1%
Power factor (Error difference not %)	<10%	±0.1
	10-20%	±0.025
	20-100%	±0.01
AC input voltage	0-100%	±1%
output voltage	0-100%	±0.5%
output current	10-20%	±10%
	20-50%	±5%
	50-100%	±1%
output power	<10%	±25W
	10-20%	±3%

	20-100%	±2%
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4.3 Blackbox Function

For the following section please refer to the latest Communication Specification for detailed information. The black box function shall store key important data to be used when a fault occurs.

- Must store data in memory and be able to withstand several read/write cycles
- PSU must be able to store failure data before the PSU turns off/fails even in catastrophic failure events both on primary and secondary side. Hold up time of the blackbox microcontroller must be able to store all the information and then shutdown.
- Last 4 events stored in memory.
- AC input current, AC input voltage, Input Power, Power factor, iTHD, DC output voltage, DC output current,
- Temperature readings, fan Speed, input voltage, output voltage, bulk voltage, various error codes from all the different converters (OTP, OVP, OCP,UVP), and warnings.
- Total run time of PSU
- Run time since last turn on
- Real time stamping
- Number of AC power cycles
- Number of AC outages (can be determined by going into backup without counting the battery test conditions)

Power supply event data is saved to the Black Box for the following events: 📄

Any events that caused the Main Output to shut down:

- Main Output over voltage fault
- Main Output under voltage fault
- Main Output over current fault
- Main Output short circuit fault
- Fan failure
- Over temperature fault 📄

Any events that caused the AC input to be bad:

- AC Input under voltage fault
- AC Input over voltage fault
- AC Input out of range frequency fault 📄

4.3.1 Fault Log History

The FAULT_LOG_HISTORY is used to read the event data of the unit. The fault log history data stores up to 4 event data sets. If the event data sets exceed 4, the oldest data set shall be removed to give way for the latest data set. Unused history data sets shall have a value of zero for all registers.

5. Environment

5.1 Temperature

- Operational or cold aisle (inlet) temperature: -5C to +45C
- Non-operational: -40C to +85C

5.2 Humidity

- Operational : 10-90% RH non-condensing
- Non-operational : 5-93% RH non-condensing

5.3 Altitude

- Operational : 0-3050m
- Non-operational : 0-12000m

5.4 Acoustic Noise

- Target sound pressure should not exceed 85dBA when fan modules are running at full speed and operating within the defined environmental envelope

5.5 Vibration and Shock (non-packaged)

The PSU shall meet vibration and shock test per EN 60068-2-6 and 60068-2-27, respectively, for both non-operating and operating condition, with the specifications listed below. The test should be performed inside the power shelf with all 6 PSUs and PMI installed. During operating vibration and shock tests, the PSU shall exhibit full compliance to the specification without any electrical discontinuities.

During the non-operating tests, no damages of any kinds (included physical damages) should occur and they should not corrupt the functionalities of the PSU per the specifications.

Shock and Vibration tests are to be performed on soft tooled and hard tooled parts.

Vibration Non-Operating:

Excitation Mode:	Sinusoidal
Test Frequency:	5Hz to 500Hz (5.0-9.0Hz) 6mm peak to peak (9.0-500.0Hz) 1g
Amplitude:	1g
Frequency Change Rate:	1 octave / min
Test Directions:	3 directions in space (x,y,z)
Duration:	10 sweep cycles for each direction (2hours 13 minutes)
Test Temperature:	Room temperature
Electrical Work:	none

Shock Non-Operating:

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Shock Pulse:	half sinus
Shock duration:	11ms
Shock Amplitude:	12g
Test Directions:	6 directions
Number of Shocks:	60 (10 per each direction)
Test Temperature:	Room temperature
Electrical Work:	None

Vibration Operating:

Excitation Mode:	Sinusoidal
Test Frequency:	5Hz to 500Hz (5.0-9.0Hz) 6mm peak to peak (9.0-500.0Hz) 1g
Amplitude:	0.5g
Frequency Change Rate:	1 octave / min
Test Directions:	3 directions in space (x,y,z)
Duration:	10 sweep cycles for each direction (2hours 13 minutes)
Test Temperature:	Room temperature
Electrical Work:	Power supply in operation

Shock Operating:

Shock Pulse:	half sinus
Shock duration:	11ms

Shock Amplitude:	6g
Test Directions:	6 directions
Number of Shocks:	30 (5 per each direction)
Test Temperature:	Room temperature
Electrical Work:	Power supply in operation

5.6 Package Vibration, Drop and Compression

PSU units in their package shall meet the following requirements:

Package Vibration	1.146 G_{rms} , 2-200-2 Hz, all three axes, Random Vibe	ISTA 3E 06-06
Package Drop	8-inch drop	ISTA 3E 06-06
Package Compression	Maximum compression loading on a bulk pack	ASTM D 642-94

6. Thermal

6.1 Operational

6.1.1 **Airflow direction:** Front-to-back

6.1.2 **DeltaT:** This is the air-side temperature difference across the rectifier assembly and represents airflow usage (CFM) in relation to heat loss in the device (W). Efficient use of airflow is critical to meeting facility-level requirements, and the following temperature difference targets are outlined.

Temperature difference $\geq 22^{\circ}\text{F}$ across 30~85% load range and up to 35°C inlet/ambient and 3050m (10,000ft) above sea-level

6.1.3 **Thermal margin:** While efficient use of airflow is important for thermal design, reserving adequate margins on components is equally critical. These margins should be defined with respect to de-rated values, as appropriate. Requirements are as follows.

Component thermal margin of $\geq 7\%$ or $\geq 5^{\circ}\text{C}$ under worst-case condition (100% load, input voltage lowest, output voltage lowest) and up to 30°C inlet/ambient and 3050m (10,000ft) above sea-level. Target whichever margin value is larger.

Component thermal margin of $\geq 4\%$ or $\geq 3^{\circ}\text{C}$ under worst-case condition (100% load, input voltage lowest, output voltage lowest), at greater than 30°C inlet/ambient and up to 3050m (10,000ft) above sea-level. Target whichever margin value is larger.

Margin to de-rated temperatures should account for associated differences in reading and measurement location. Impact to reliability should also be considered when determining required margin.

6.2 Thermal design requirements

- 6.2.1 **Sensor accuracy:** For discrete and critical sensors (such as ambient temperature), an accuracy of $\pm 2^{\circ}\text{C}$ is required ($\leq \pm 1^{\circ}\text{C}$ is preferred). Exhaust and inlet temperature sensors are required in the unit. If a component does not have an integrated temperature sensor, and uses a proxy, need to target an accuracy $\leq \pm 5^{\circ}\text{C}$ ($\leq \pm 2^{\circ}\text{C}$ is preferred). If this component is temperature sensitive, thermal margin requirements defined above should account for sensor inaccuracy.
- 6.2.2 **System fan:** Should be sized to support operation across environmental and loading envelopes, with an adequate operating range (speed) to achieve requirements outlined in this document. The fan should also have adequate overhead to accommodate back-pressure resulting from shelf design, rack-level accessories and data center operation. In general, head room to overcome a back-pressure of ≥ 0.3 inches of water is highly recommended. When the rectifier is plugged in, the fan should stay operational irrespective of load and maintain front-to-back airflow direction (overcome potential back-pressure). Mounting of the fan must meet any vibration and acoustic criteria and should not violate any physical constraints outlined. The fan should be included within the power supply enclosure.
- 6.2.3 **Surface temperature:** To make the rectifier assembly safe for handling in-operation, accessible surfaces should not exceed a temperature of 70°C .

6.3 Fan Failure

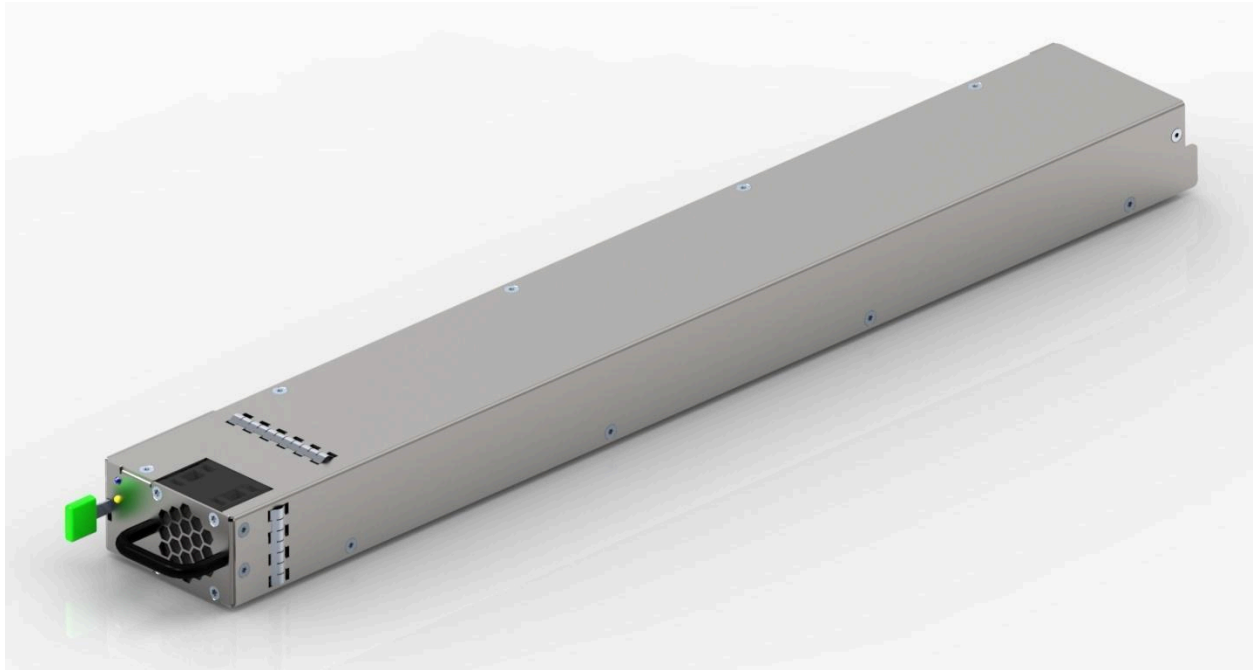
If a fan fails, the rectifier must indicate the failure with a signal that will be reported via software as well as an LED indicator on the front panel. The rectifier shall not need to shut down because of a failed fan and only shut down if there is a fault, i.e. over-temperature fault.

6.4 Rectifier Thermal Monitoring

Each rectifier shall provide the following parameters via the defined communication protocol (in addition to monitoring of rectifier components and operating parameters). The following thermal parameters must be available for each rectifier and labeled accordingly:

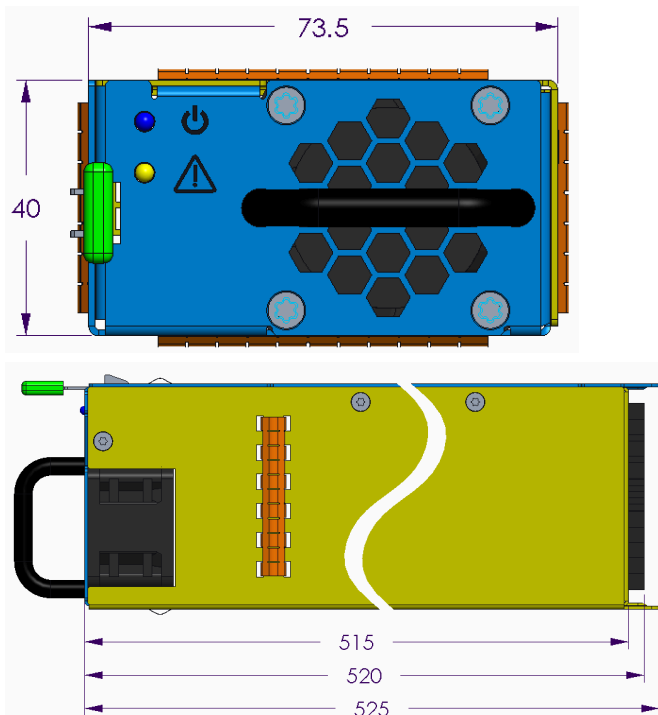
- Inlet temperature
- Exhaust temperature
- Fan RPM (average, if >1 fan used in the rectifiers); percent is acceptable as long as full speed rpm is provided at some point
- Fan fail signals

7. Mechanical



7.1 PSU Physical Dimensions

The PSU rectifier size is 73.5mm x 40mm x 525mm [Width x Height x Depth]



7.2 Construction

The PSU base and cover shall be assembled using flathead screws. No rivets are allowed as the PSU must have the ability to be opened using a screwdriver. The individual base and cover can be welded, riveted or screwed together, consistent with meeting shock and vibration requirements. There shall be no sharp corners or edges.

The sheet metal material shall be steel, pre-plated hot-dip zinc coated, with .8-1mm of thickness.

7.3 Materials and Fasteners

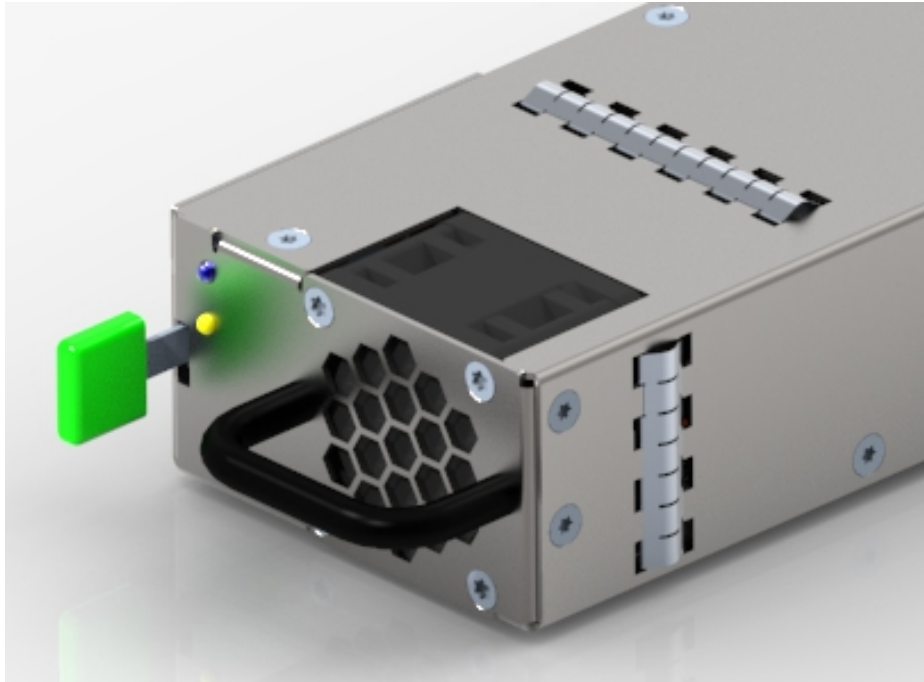
The sheet metal material shall be steel, pre-plated hot-dip zinc coated, with 0.8mm – 1.0mm of thickness unless otherwise specified. Any plastic material used should meet UL 94-V0 specifications. It is highly suggested to use PCR (post-consumer recycled) plastic. The following PCR plastics have been qualified for use:

- GLite MBS-200BKR01
- GLite MBS-200GNR01
- Kingfa JH960-6950 C2B-S0759
- Kingfa JH960-6950 C7G-S0023
- Wistron WAM NCT50T##

7.4 Latch & Handle Requirements

A latch and handle are required for PSU removal. The latch shall be attached in the location shown on the mechanical drawing, to interface with the cutout in the chassis. The latch design may vary, but the finger interface of the latch must be Pantone 375C (Green).

A foldable handle is highly suggested. The handle shall be designed so that it does not protrude past the top and bottom surfaces when folded 90°. Handle touch points to be Pantone 375C (Green). Please note that the PSU will be heavy, and the handle should be sturdy enough to carry the entire weight of the PSU.



7.5 EMI Gaskets

EMI gaskets are to be placed on the left & right and/or top & bottom sides of the PSU. The main purpose of the gaskets is for PSU module to shelf grounding and secondary purpose is for EMI containment. Gaskets are to be placed towards the front of the PSU module so they make full contact with the walls of the PSU shelf.

Suggested placement distance from front panel along length of BBU module:

Right/Left Side: 15mm-25mm

Top/Bottom Sides: 5-15mm (Assuming no fan interference), 55mm-105mm.

7.6 Chassis Interface

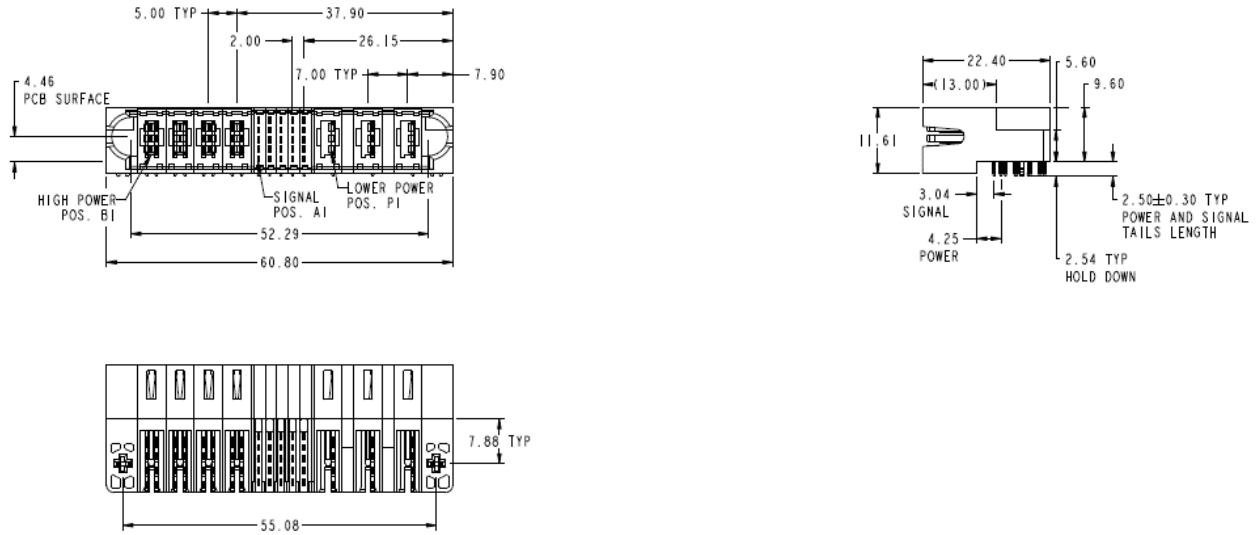
The handle of the rectifier may not protrude from the front surface of the rectifier by more than 23mm. The latch shall be located on the left side of the rectifier and interface with a rectangular hole in the chassis wall. Please refer to the 3D drawing for latch location on the rectifier. They should only lock into place when good electrical contact is made on the rear blind mate connectors. This scheme will allow a quick installation of the Power Supply in the tray, and without the need of using a screwdriver.

7.7 Rear Blind Mate Connector

The rear blind mate connector of the PSU shall be Amphenol 10127396-01U1520LF or equivalent. This is a R/A plug, PwrBlade ULTRA HD connector with 4 high power pins, 25 signal pins, and 3 low power pins. Please refer to the drawing for more details.

The connector position within the PSU is fixed in X, Y, and Z direction according to the 3D drawing. This cannot be altered due to mix-and-match requirements for the power supplies into the shelf.

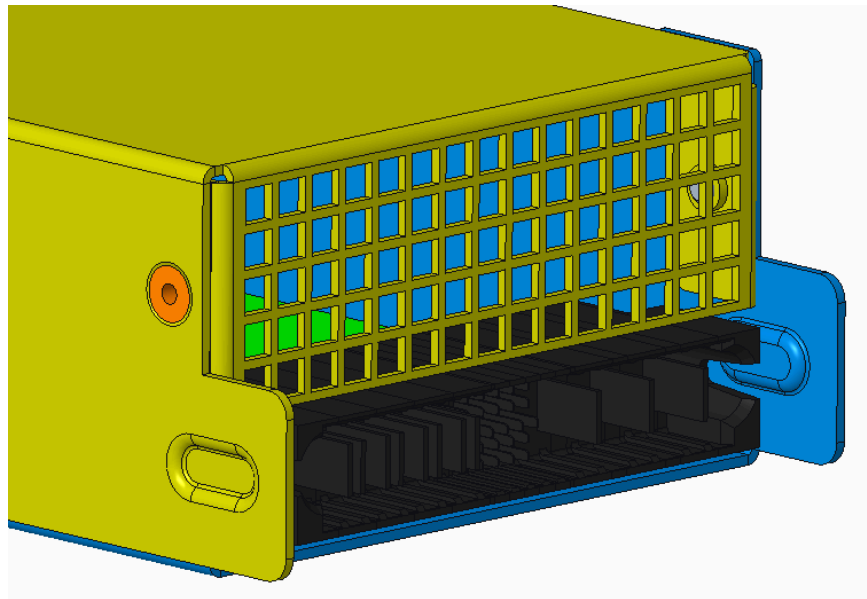
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7.8 Rear Blind Mate Connector Protection

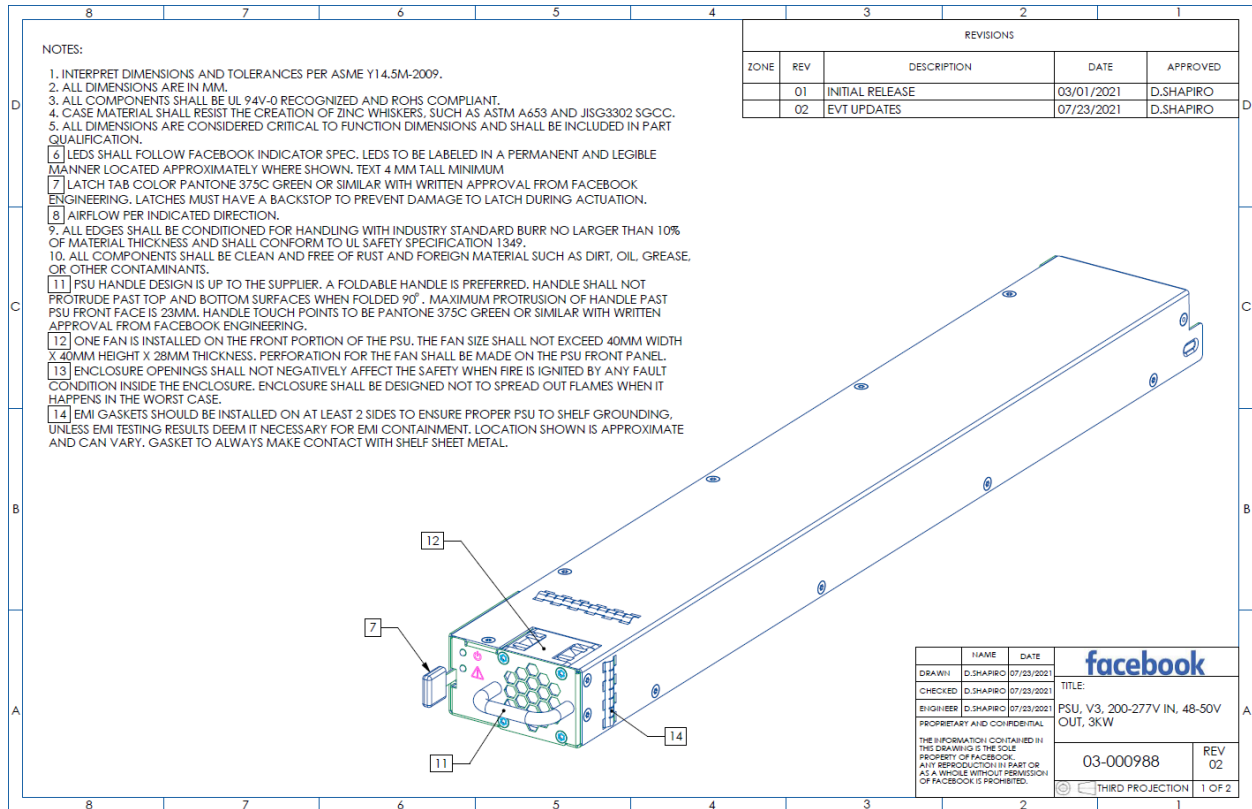
A method of protecting the rear blind mate connector on the PSU is required to prevent damage from accidental mishandling during manufacturing or end user handling of the module. Please review mechanical 3D CAD for reference design of protection tabs. These tabs should not interfere with any features on the PSU Shelf.

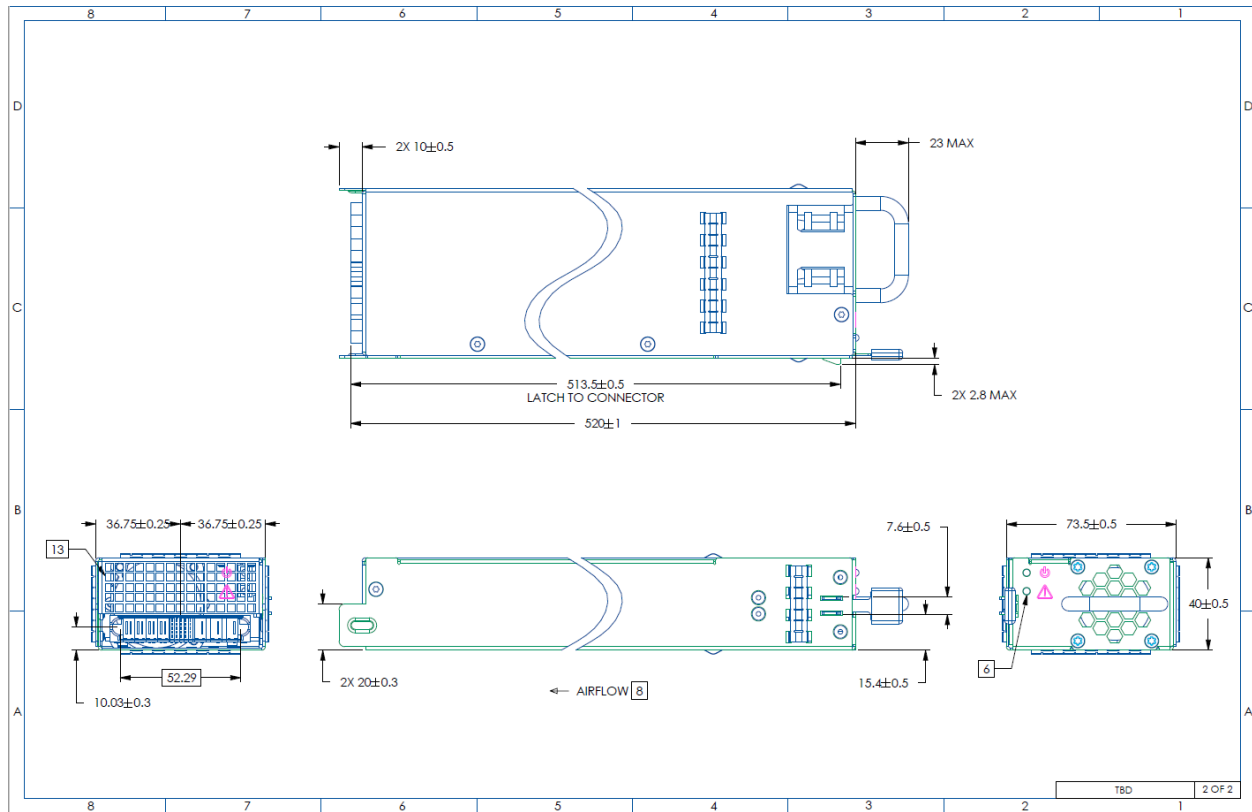
These tabs also double as a keying mechanism to prevent the PSU from being installed upside down.



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7.9 Mechanical Drawings





8. Reliability and Quality

8.1 Derating Design

A comprehensive stress analysis and derating design shall be performed for the rectifier. The stress analysis shall include electrical, thermal, and mechanical stresses with actual measurements. The components in the rectifier design shall be properly derated and to meet the derating guideline as specified in IPC-9592B “Requirements for Power Conversion Devices for the Computer and Telecommunication Industries”, Appendix A or supplier’s own derating guideline.

8.2 MTBF Requirements

Vendor shall provide Calculated MTBF using Telcordia SR-332 latest version (Method 1 Case 1/Parts Count in EVT and Method 1 Case 3/Parts stress in DVT). Target MTBF is 500K hours and calculation should be at 45°C of ambient temperature, 277Vac of input voltage, and 100% load. The fan is not included (MTBF of the fan will be provided separately).

The PSU shall meet a demonstrated MTBF of minimum 500K hours at 90% confidence level prior to first customer shipment (Pilots samples, Mass Production units). DMTBF is to be performed with PSUs installed in the shelf using PSUs and power shelves from mix-source build.

MTBF goal: the Vendor shall provide to Facebook the best MTBF numbers that the PSU will be able to meet, no matter the minimum requested. Facebook will use this information for an overall reliability study of the whole system.

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The fan L10 life shall be at least 5 years at 45°C inlet air temp and full speed (to be verified with the fan vendor)

8.3 Design Failure Mode and Effect Analysis (DFMEA)

A comprehensive DFMEA shall be performed for the rectifier. The DFMEA report shall include a list of critical components, risk areas, and corrective actions taken.

8.4 High Accelerated Life Test (HALT)

A comprehensive HALT shall be performed on the rectifiers. The HALT equipment, testing procedure, sample size, testing report and documentation, and root cause analysis and corrective action requirements shall follow the requirements as specified in IPC-9592B, Section 5.2.3 and Appendix D.

HALT test is to be performed on PSU samples from mix-source build.

8.5 Burn-In (BI) and Ongoing Reliability Testing (ORT)

Either 100% burn-in or 100% HASS (Highly Accelerated Stress Screening) test shall be performed at the beginning of the rectifier mass production. Either BI or HASS could be chosen based on supplier's capability and preference.

The detailed requirements for BI and HASS test durations, duration reduction plan, and test profile shall follow the requirements as specified in IPC-9592B, Appendix E for Category 1 PCD products.

After meeting the acceptable failure rate criteria as listed in Table E-1 of IPC-9592B Appendix E, the 100% BI or HASS could be reduced to sampling BI or HASA.

Ongoing Reliability Testing (ORT) shall be performed on the rectifiers when BI or HASS test is reduced from 100% to sampling and when BI or HASS is eliminated after at least one (1) year. The detailed ORT plan and requirements shall follow the requirements as specified in IPC-9592B, Appendix E, Section E.2.3.

8.6 Other Reliability Tests

The following tests shall be performed on PSU samples from mix-source build per procedures, test conditions, and test sample size as specified in sections 5.2.4, 5.2.6, and 5.2.7 of IPC-9592B.

- Temperature, Humidity, and Bias (THB)
- Temperature Cycling Test (TC)
- Power and Temperature Cycling Test (PTC)

8.7 Disallowed Components

Facebook reserves the right to select some preferred/mandatory parts, during the development phase (selection of an approved vendor list (AVL) subset). The Vendor will work with Facebook to solve system integration problems, should any issues arise.

- Trimmers and/or potentiometers.
- Tantalum capacitors.
- Dip switches.
- High side driver ICs
- Paralleled power MOS are allowed provided that the design prevents parasitic oscillations

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- SMT ceramic capacitors are allowed with the case size < 1206. The size 1206 can still be used when SMT capacitors are placed far from the PCBs edge, and with a correct orientation that minimizes risks of cracks [any size > 1206 must be highlighted to Facebook during DFM review].
- Allowed ceramics materials for SMT capacitors are: X7R or better material. The COG or NPO types should be used in critical portions of the design, such as feedback loop, PWM clock settings, etc. [any changes shall be highlighted and brought up during DFM review].
- Relays: the use of any electro-mechanical relays, and type shall be discussed up front before any approval is given include them in the design.
- Resistors by Royal Ohm are not to be used.
- Facebook will approve all control ICs.
 - **8.7.1 Capacitors**
 - All the electrolytic capacitors shall be rated at 105°C 500V and shall be selected from Japanese and US manufactures only.
 - All capacitors shall have a predicted life of at least 5 years at 45°C inlet air temperature under worst conditions.
 - **8.7.2 Sheet Metal Material and Zinc Whisker Implications**
 - Sheet Metal Chassis Material is hot-dip Zinc coated, JIS G3302
 - SGCC (Z18 to Z22), with 0.8mm - 1mm of thickness. The 'Z' parameter defines the metal coating thickness: Z20 is for 40µm of thickness, and Z22 is for 43µm.
 - The Japanese standard is 'JIS G3302', while the US standard is 'ASTM A653'.
 - Mechanical design shall prevent sharp edges and possible metal oxidation in the critical points of the sheet metal (e.g. in the cut & bends portions, etc.).
 - Both chassis design and metal base material will not promote the growth and propagation of zinc and tin whiskers.
 - Metal base materials with electro-zinc plating, or poor conductivity plating, are not allowed.
 - Alloy materials are a possible option, while stainless steel is another possibility provided that it makes cost sense (both options are subject to Facebook approval)
 - Aluminum material is not allowed for the enclosures.
- The chassis enclosure, as well as the whole electronics, shall meet certain contamination requirements (see ANSI/ISA 71.04 G1).

8.8 Manufacturing Quality and Production Tests

It is required to meet the quality process requirements as specified in IPC-9592B, Section 6 ("Quality Process"), which include PFMEA, statistical process control (SPC), corrective action process, yield control, materials traceability, product change notice (PCN), qualification of change, etc.

8.8.1 Burn-In (BI) and Ongoing Reliability Testing (ORT)

Either 100% burn-in or 100% HASS (Highly Accelerated Stress Screening) test shall be performed at the beginning of the rectifier mass production. Either BI or HASS could be chosen based on supplier's

capability and preference.

The detailed requirements for BI and HASS test durations, duration reduction plan, and test profile shall follow the requirements as specified in IPC-9592B, Appendix E for Category 1 PCD products.

After meeting the acceptable failure rate criteria as listed in Table E-1 of IPC-9592B Appendix E, the 100% BI or HASS could be reduced to sampling BI or HASA.

Ongoing Reliability Testing (ORT) shall be performed on the rectifiers when BI or HASS test is reduced from 100% to sampling and when BI or HASS is eliminated after at least one (1) year. The detailed ORT plan and requirements shall follow the requirements as specified in IPC-9592B, Appendix E, Section E.2.3.

8.8.2 Hipot and Ground Continuity Test

The PSU shall be tested 100% in production for both Hi-Pot (with the applicable limits for the AC leakage current) and ground continuity (per the applicable standard). Stamps shall be applied to the chassis proving that both tests passed in productions.

8.8.3 DFT and DFM

- The Vendor shall provide DFT and DFM reports at EVT and/or DVT phase.
- For all the boards used in the PSU design: the in-circuit test coverage and test point access shall be > 95% or higher.

8.8.4 Quality Control Process

- All assembly inspection dimensions and tolerances in the drawings provided must be met.
- Incoming Quality: <0.1% rejections.
- CPK values should equal or exceed 1.33 (Pilot Build and Production) using a sample size equal to 32 for CPK measurement.
- CPK measurement should be performed on every batch/lot build of pilot and mass production. During production, weekly CPK reports must be sent to Facebook engineering team.
- The Vendor will implement a further quality control procedure during production, by sampling power supplies randomly from the production line and running full test to prove ongoing compliance to the requirements (it may include EMI production). Process shall be documented and submitted to Facebook prior to production. The relative reports will be ongoing submitted to Facebook.
- The vendor will propose to Facebook, for audit and approval, ongoing burn-in procedure to be used in production, that will not start without an agreement on some sort of burn-in procedure
- PCB boards are UL recognized components rated 94 V-0 and rated 130°C MOT.
- Multi-layers (> 2 layers) PCB boards are welcome for a better layout and simplification of the manufacturing process, however if they make sense for cost.

8.8.5 Mass Production First Article Samples

Prior to final project release and mass production, the Vendor will submit to Facebook a good quantity (70) of PVT production pilot run verification samples, including the following documentation:

- All the pertinent development docs, production docs, and reports necessary to Facebook to release the product for mass production.

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- The pilot samples shall be built in the allocated facility for mass production and use hardtooled chassis and parts (where applicable).
- Full spec compliance matrix, full test report, production line final test 'pass' tickets.
- Samples passed the burn in process planned for production.
- Samples are shipped using the approved for production shipping box.
- The units are certified and safety label is applied ("Pending Certification" sticker may be allowed until the certification process is complete).

8.9 Spec Compliance, Quality FA, Warranty

- The Vendor is responsible for the PSU to meet the specifications as stand-alone unit as well as at system level, and for assuring that the power supplies shipped in production will conform to the specifications with no deviations.
- A specification compliance matrix and test report shall be submitted to Facebook for each PSU revision: EVT(P1), DVT(P2), and PVT (Pilot).
- The Vendor is responsible to exceed production quality standards achieved on the pilot run built without fluctuations.
- All failures from EVT, DVT, PVT are required to complete failure and root cause analysis and report corrective action prior to entering mass production.
- Failure analysis on defective RMA units shall be provided to Facebook with corrective action plan, within two weeks from when the units are received at the Vendor's facility.
- The Vendor shall warrant the power supply for defects and workmanship for a period of three (3) years from the date of shipment when the device is operated within specifications. The warranty is fully transferable to any end user. A standard "VOID" warranty sticker may be applied.

8.10 Mix-source Builds

Suppliers are required to conduct a mix-source build ideally at DVT using prime and 2nd source/alternate parts in the BOM. Samples from mix-source builds are to be used in all Reliability and Environmental tests for the power supply as would be applicable.

8.11 Conformal Coating

The gate terminals of all high-voltage MOSFETs as well as the most sensitive areas of the electronic circuitry in the boards must be protected against potential resistive contacts with other voltage potentials (e.g. MOS Drain leads, etc.) due to whiskers, pollutant particles, dust, moisture (for example contaminant substances can become conductive in presence of moisture), and up to some local wet condensation occurrences.

Local automated, conformal coating shall be applied to critical areas of the boards to protect sensitive circuitries, using an atomized spray process (no dipping process is considered here). The thickness of the coating shall be ~50µm to ~150µm. The Vendor (mainly the ultimate Manufacturing Facility) shall demonstrate to possess good skills, experience, and long years of experience on automated conformal coating application and process. The power modules main board shall be

partially conformal coated (top & bottom); critical board areas shall be agreed upon, typically the ac high-voltage input section at shelf level, like the AC input, board-mount connector area.

9. Compliance requirements

The power supply unit shall be designed for compliance to allow worldwide deployment. Additionally, the manufacturer is fully responsible for:

- ensuring the complete compliance of the power supply shelf in the environment it is intended to function (as described by the Rack Spec)
- maintaining and updating the power supply shelf safety reports to current requirements and all new released requirements.
- all design and recertification costs required to update the power supply to meet the new requirements.
- Meeting EMC requirements
- Meeting Safety requirements

The manufacturer is responsible for obtaining the safety certifications specified below.

9.1 Safety Standards

The product is to be designed to comply with the latest edition, revision, and amendment of the following standards. The product shall be designed such that the end user could obtain the safety certifications: UL 62368-1, IEC 62368-1 and EN 62368-1; hazard-based performance standard for Audio video, IT & Communication Technology Equipment

The manufacturer shall obtain the following safety certifications for the power supply shelf as applicable. Only requirements that absolutely rely on or are affected by the system may be left to the system level evaluation [i.e. minimize Conditions of Acceptability]. Below are common requirements for North America and Europe. For other countries, different certifications may be required:

- UL or an equivalent NRTL for the US with follow-up service (e.g. UL or CSA).
- CB Certificate and test report issued by CSA, UL, VDE, TUV or DEMKO
- CE Marking for EU

9.1.1 Component Safety requirements

Following are the safety requirements for major components:

- All Fans shall have the minimum certifications: UL and TUV or VDE.
- All current limiting devices shall have UL and TUV or VDE certifications and shall be suitable rated for the application where the device in its application complies with IEC/UL 62368-1.
- All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printed wiring board manufacturer.
- All connectors shall be UL recognized and have a UL flame rating of UL94V-0.
- All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer. SELV Cable to be rated minimum 80V, 125C.
- Product safety label must be printed on UL approved label stock and printer ribbon. Alternatively, labels can be purchased from a UL approved label manufacturer.
- The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

9.2 EMC Requirements

The power supply shall meet the following requirements in the latest edition of standards when operating under typical load conditions and with all ports fully loaded;

The Power supply integrated into the shelf is called the component power supply. Manufacturer shall provide the proof of compliance for the component power supply that are required for spare parts shipment. The component power supply shall not contribute any noncompliant conditions to the end-use product.

If at any time it is found that a supplier's component power supply causes the end-use product to fail emissions and/or immunity testing, the supplier will be instructed to investigate and resolve the problem. The power shelf shall have minimum 6dB margin from the Class A limit for the radiated and conducted emissions. Depending on the system manufacturer's design goals and business needs, more margin may be required when it is integrated into the final end system.

The following EMC Standards (the latest version) are applicable to the product.

- FCC /ICES-003
- CISPR 32/EN55032
- CISPR 35/EN55035 - Immunity
- EN61000-3-2 - Harmonics
- EN61000-3-3 - Voltage Flicker
- VCCI
- KN 32 and KN35

Each individual basic standard for immunity test has the following minimum passing requirement. Higher level of passing criteria may be applied depending on the system manufacturer's design goals and business needs.

- EN61000-4-2 Electrostatic Discharge Immunity
 - Contact discharge: >5.6kV
 - Air discharge: >11.2kV
- EN61000-4-3 Radiated Immunity
 - > 3V/m
- EN61000-4-4 Electrical Fast Transient Immunity
 - AC Power Line: >1kV
 - Signal Line: >0.5kV
- EN61000-4-5 Surge
 - AC Power Line: >2kV (Line-to-line), >4kV (Line-to-earth)
 - Signal Port: >1kV
- EN61000-4-6 Immunity to Conducted Disturbances
 - DC Power Line: > 3Vrms
- EN61000-4-8 Power Frequency Magnetic Field Immunity, when applicable
 - > 1A/m
- EN61000-4-11 Voltage dip and sag

9.3 Environmental Compliance

The power shelf (including all components inside) shall comply with the following minimum environmental requirement and manufacturer shall provide full material disclosure, Declaration of Conformity and technical documentations to demonstrate compliance. The system manufacture may have additional requirements depending on its design goals and business needs.

- RoHS Directive (2011/65/EU and 2015/863/EU); aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture
- REACH Regulation (EC) No 1907/2006; registration with the European Chemicals Agency (ECHA), evaluation, authorization and restriction of chemicals.

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- Halogen Free: IEC 61249-2-21, Definition of Halogen Free, 900ppm for Br or Cl, or 1500ppm combined
- US SEC conflict mineral regulation to source mineral materials from socially responsible countries, if applicable
- Waste Electrical and Electronic Equipment (“**WEEE**”) Directive (2012/19/EU) if applicable; aims to reduce the environmental impact of EEE by restricting the use of certain substances during manufacture
- The vendor shall provide the declaration of compliance document stating that a product doesn't contain any substances regulated by EPA 40 CFR751. Refer to FBPN: 18-000142 for more detail environmental compliance requirements

9.4 Documentation

The manufacturer shall provide reproducible copies of all pertinent documentation relating to the following:

- Product Information
- Bill of Materials
- Schematics
- functional test report
- Final Compliance Approval
- NRTL certificate and report, Conditions of Acceptability and test report plus User documentation that explains safe installation and operating procedures.
- CB Certificate and report, including schematics
- Manufacturer's Declaration of Conformity to EN 62368-1, EN55032, EN55035 and ROHS
- FCC Part 15 Class A and CISPR32 Class A test data
- Declaration of Conformity to EN 61000-3-2 Class A and test report including waveforms and harmonic output levels.
- Other applicable certificates required by the system manufacturer.

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Attachment A: Power Supply Impedance Specification

See attached doc.