VI and CV Tests

EDIT 2024

Goals:

- Characterize device leakage current
- Measure depletion voltage

Devices:

- 290 micron diodes (Hamamatsu CMS OT 2S) p-type: n-on-p sensors (n+ implants on p-type substrate); 290 micron active thickness with an extra 30 micron thick backplane; high resistivity Float-Zone process with bulk resistivity 3.5-8 kΩcm

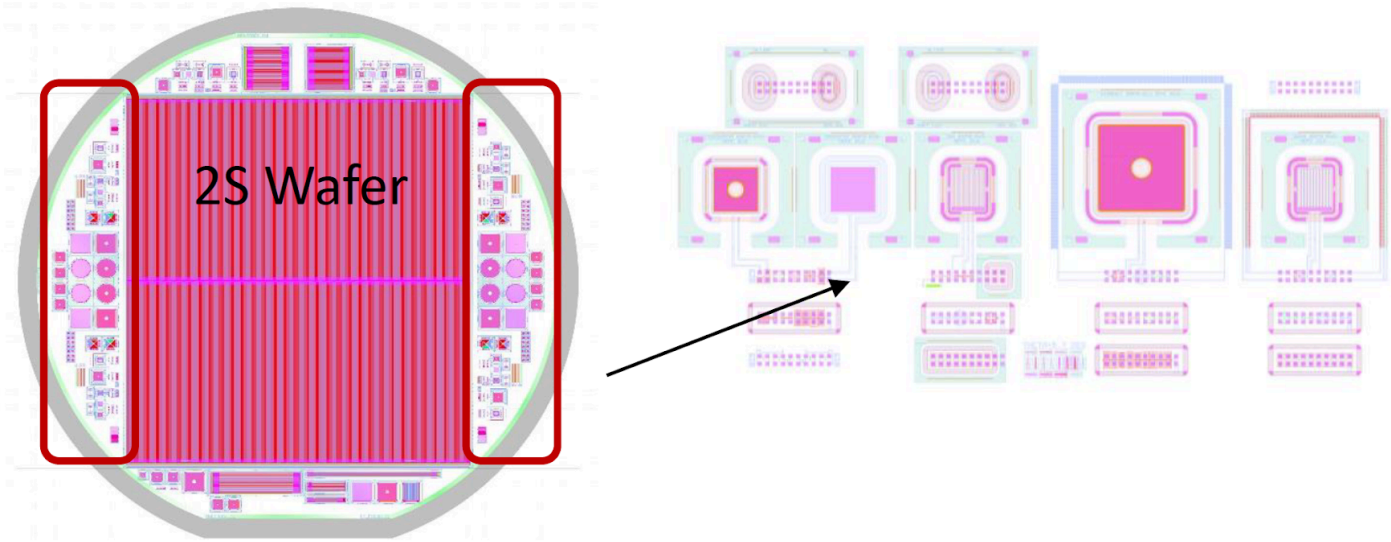


Figure 1 Layout of a CMS Outer Tracker 2S silicon wafer and part of one of the "halfmoons"

Test suite:

- Voltage source/measure unit (2410)
- LCR meter (HP4284A) – measures inductance (L), capacitance (C) and resistance (R)
- GUI running on a laptop to control and monitor data from above.
- VI diode

- CV for diodes (map depletion voltage)

Test Software

The tests will be performed using a GUI that can be used for both IV and CV tests. A screen capture of the GUI is shown below. The tests can be configured to vary the maximum voltage and voltage step, the compliance (maximum current), the LCR frequency and voltage, and the equipment used in the setup. An n-type sensor must have positive voltage applied to the back side, p-type uses negative backside bias.

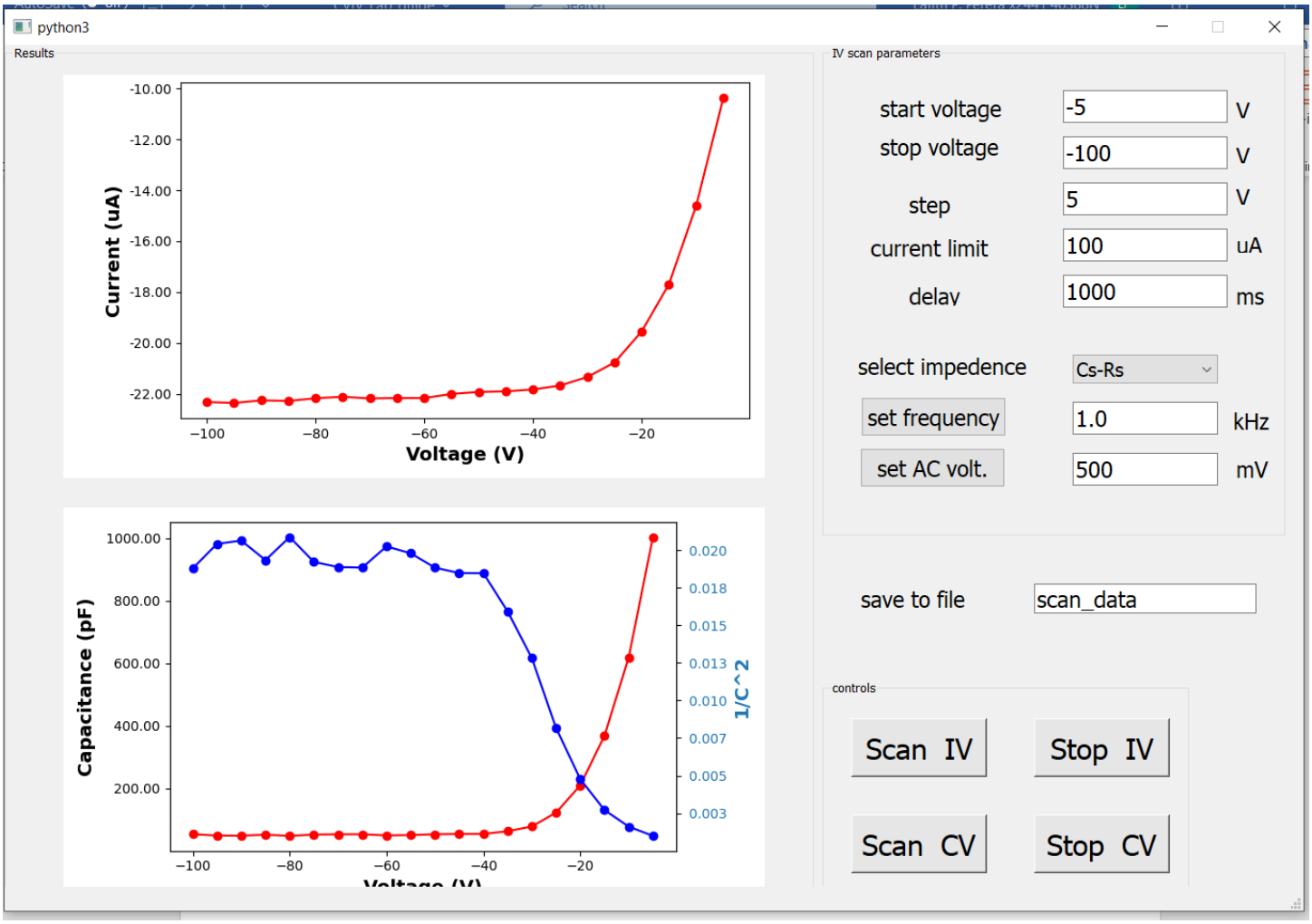


Figure 2 The GUI to run the scans

Connections

For these tests, we will use bare diodes on silicon wafers and packaged test diodes.

1) Testing using the probe station:
    a. For bare diodes, we use a probe station to make contacts with the probe station needle on the bulk of the diode.

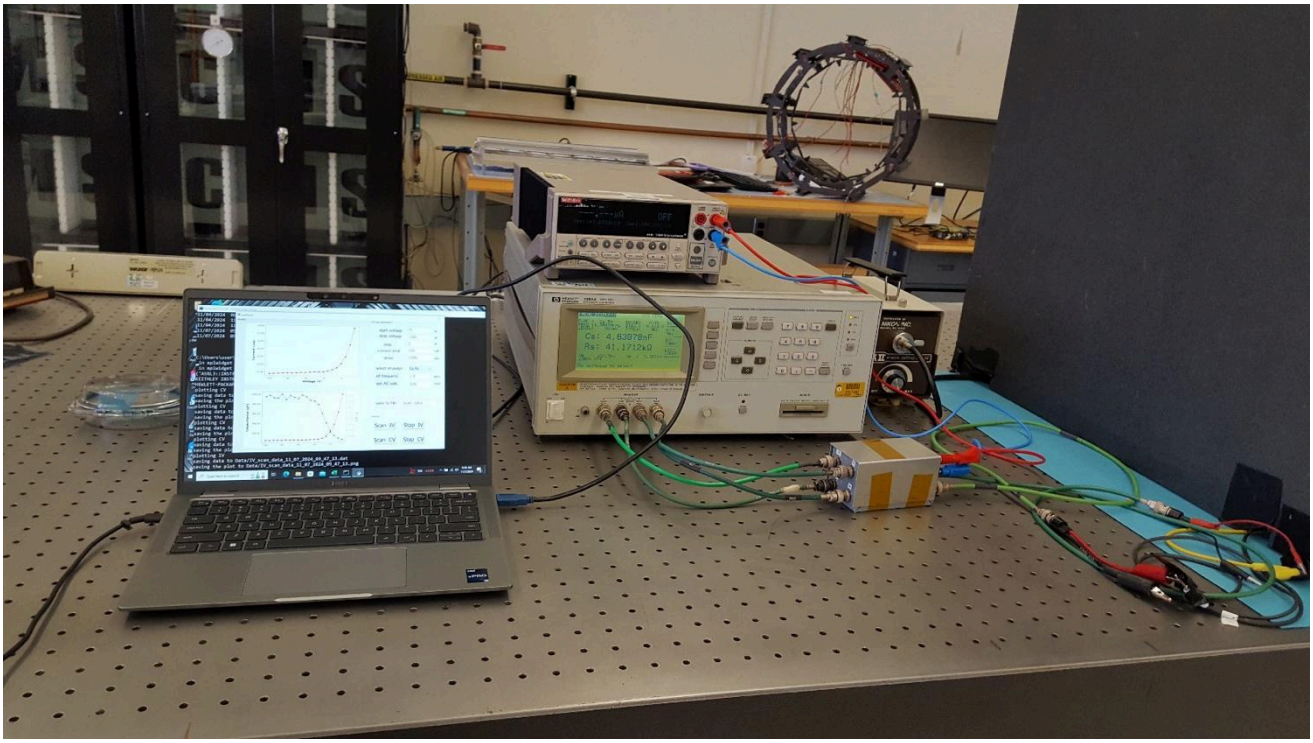


Figure 3 Test setup with LCR meter, power supply and laptop

2) Testing using the test card:
    a. The packaged diodes can be contacted with the attached connectors.
    b. The parts are packaged on test cards like this:

    • One of the three connector pins connects to the center pad on the test card via a trace in the card. The center pad uses conducting adhesive film to connect to the backside of the diode. Use a microscope to check which of the three pins has the trace connecting it to the center pad (left or right pin?).

• The sensor charge collection node is wire-bonded to the pin opposite the backside pin (right or left).

- The sensor guard ring is left floating (not connected to center pin)
- Connect the two wires in their connector to your test card and close the lid of the black box.

Test card assembly

The test card we are using is a very simple 1-layer PCB. The electrodes and the center pad are electroplated for conductivity. The group should follow these simple steps to experience the basics of silicon detector assembly:

1) **Preparing the test card:** as seen in Figure 4, the test cards come originally we many connectors mounted so that one could in principle read out up to 9 test structures. However, this poses problems for the wirebonding process, unless one wanted to use a deep-access wirebonder, which is a lot more complicated than is warranted for this exercise. If your test card has more than two connectors, you will need to remove them using a soldering iron or a heat gun.

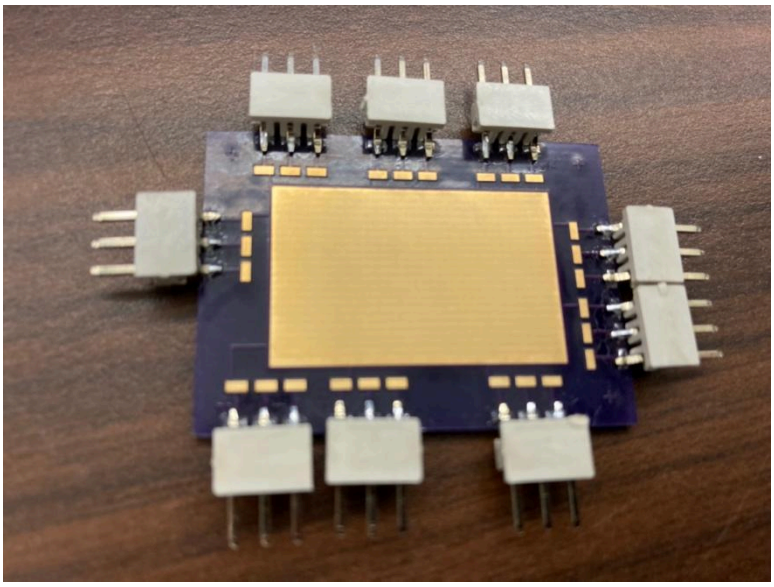


Figure 4 Bare test card before assembly

1) **Dicing the test structures:** the test structures we will be using come from the CMS HL-LHC Outer Tracker upgrade and they come embedded in so-called halfmoons (Figure 5) that have been cut from the periphery of the 2S sensor wafers. The halfmoons contain an assortment of test structures, including baby strip sensors and

various diodes and capacitors. The halfmoons are obviously too large to mount on the test card, so we need to dice them. For this and the next two steps you need to go into the cleanroom of LabD after gowning up. The lab in the cleanroom is operated by highly skilled technicians that work with us on the CMS upgrades. You will work with Bert on cutting the halfmoons until you have a small enough piece containing a diode and a capacitor (circled in red in Figure 5).

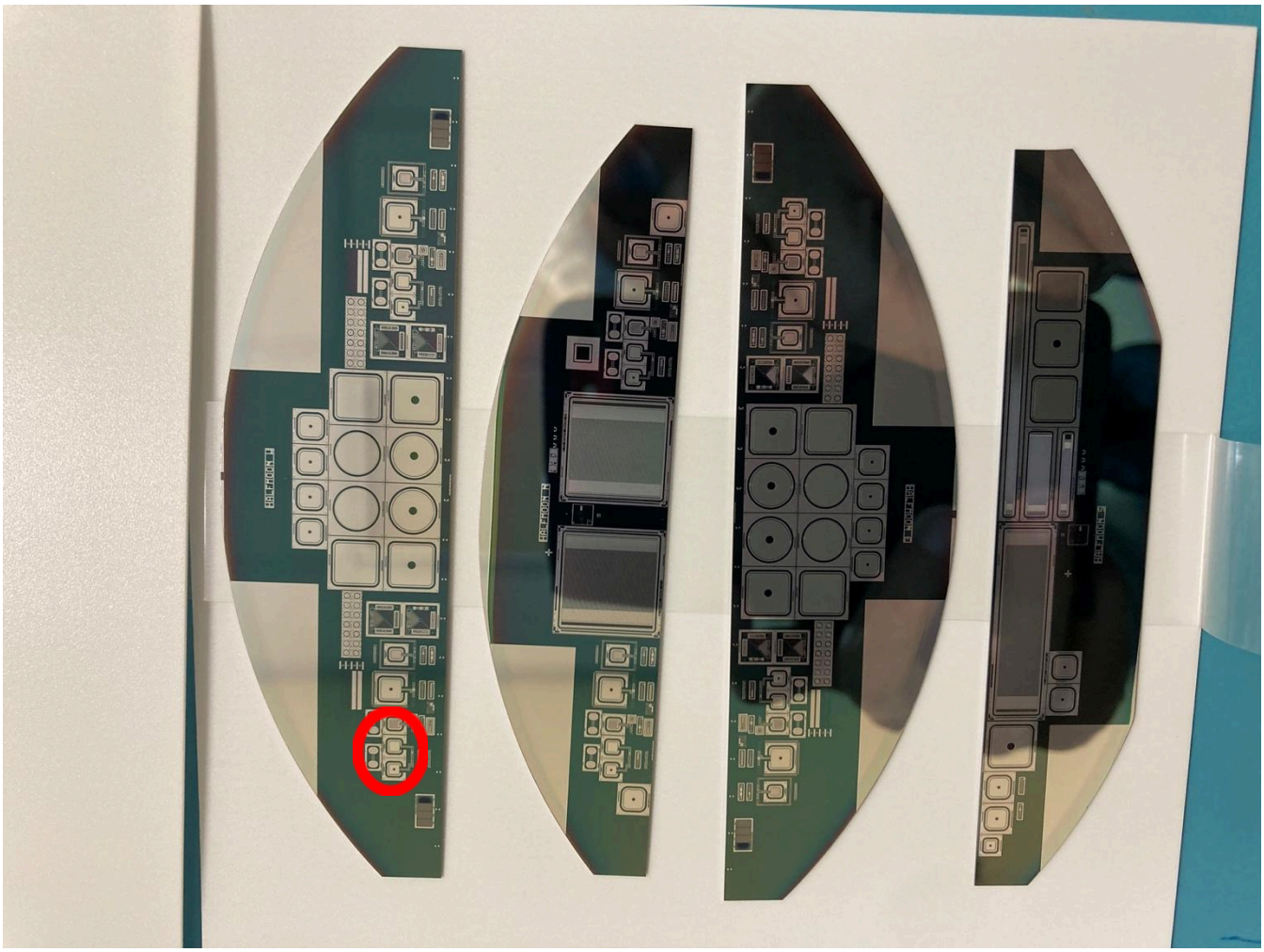


Figure 5 HL-LHC CMS Outer Tracker 2S sensor wafer halfmoons

2) **Mounting the test structure on the test card:** since we are biasing the sensors from the backside through the central conductive pad in the test card, we need to make sure we have a good electrical contact between the two. Normally we use conductive epoxy for such an assembly, but that can get messy and takes time to cure. For this small assembly we decided to use conductive adhesive tape. You will work with Bert to glue the sensor to the test card.

3) **Wirebonding:** as we said, the bias voltage arrives to the test structures through the backside of the sensor. The other half of that connection is through the top side, for which we need to connect the top side of the test structure to one of the pins on the test card via a wirebond. This will be performed by one of our wirebond technicians, Megan or Zani, but you should watch, it's quite cool.

The fully assembled test card can be seen in Figure 6. We put a 3D-printed cover on to protect the very fragile silicon and the wirebonds. **Don't stick your finger in there!**

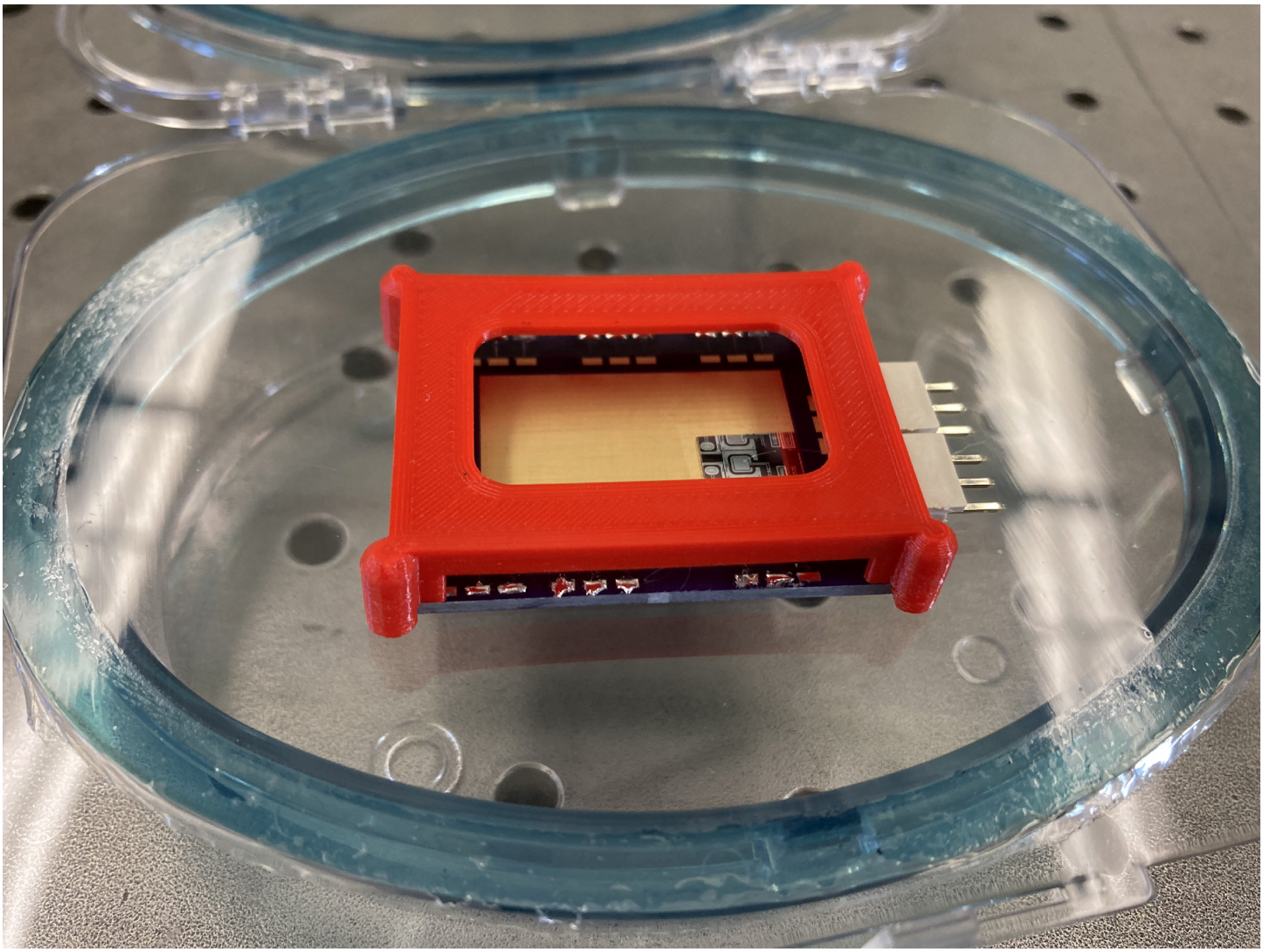


Figure 6 Fully assembled test card with two diodes wirebonded

IV Test:

The test requires a power supply with an internal pico-ammeter. The best choice is a sensitive source measurement unit (SMU) with high voltage isolation and current limitation such as a Keithley-487/237 or 2010. Connect the test structure and SMU as shown in the figure below. Measure the total leakage current between the bias rail and the sensor backside in 10V steps up to 400V with a 1 second delay between voltage increments. A current limit of 5µA must be imposed throughout the measurement. The temperature of the probe station environment should be recorded as well.

1) Connect the substrate to the voltage source (2410) high.
2) Connect probe to inner (bulk) contact (2) to voltage source low
3) Connect probe to guard ring contact (3) to voltage source low

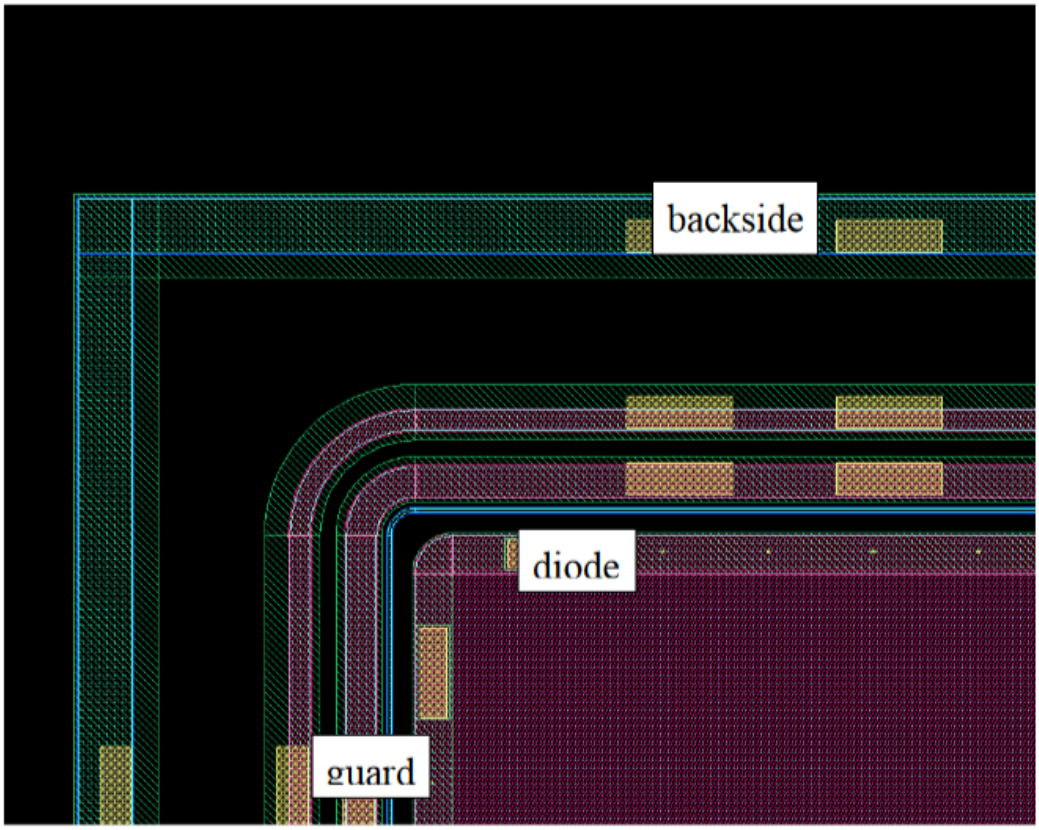


Figure 7 Schematic layout of a diode

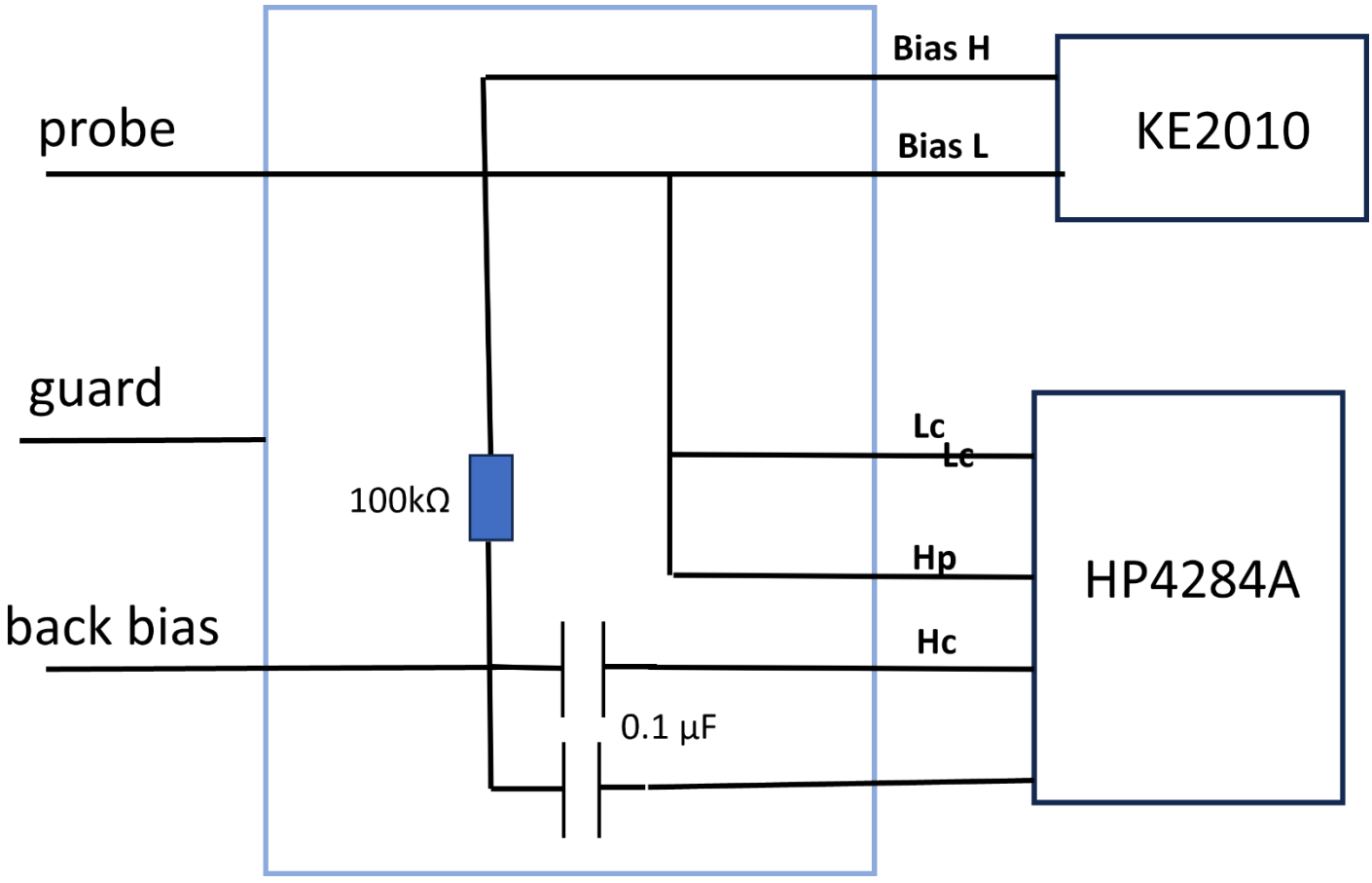
CV Test:

Connect the LCR meter, bias supply, probe, and chuck as shown in Fig. 5, with an external bias adapter. The LCR is connected through a bias box to protect the LCR from high voltage.

Measure and record the capacitance in 10V steps up to 300V with a 1-second delay between voltage increments. Use 10kHz with the LCR meter with 0.5 V amplitude. To determine the full depletion voltage (FDV), the data is plotted as 1/C2 versus bias voltage.

• Determine the full depletion voltage as the intersection between the lines drawn on the rising edge and the plateau. This may not be well-defined for some samples. Why?

• Calculate the thickness of your samples using an assumption of a parallel plate capacitor. We will provide values for the active areas.



`Bias box wiring diagram.