Roll No……..….. **Total No. of Printed Pages: [1]**
Total No. of Questions: [09]

B. Tech ECE (Semester –7th)
VLSI TECHNOLOGY
Subject Code: BECED1-731
Paper ID: [18111339]

Time: 03 Hours **Maximum Marks: 60**

Instruction for candidates:

1. Section A is compulsory. It consists of 10 parts of two marks each.
2. Section B consist of 5 questions of 5 marks each. The student has to attempt any 4 questions out of it.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

Section – A **(2 marks each)**

Q1. Attempt the following:

a) Define NMOS and CMOS IC technology.
b) What is 'bipolar IC fabrication'?
c) Explain the need of accelerated test model in VLSI.
d) Discuss molecular beam epitaxial technology.
e) Discuss the oxidation technique and system in VLSI.
f) What is the diffusion coefficient of a semiconductor?
g) Differentiate between Latches and Flip-Flops.
h) Define scattering phenomenon.
i) What is 'What is Fick's law of diffusion'?
j) Define the term Lithography.

Section – B **(5 marks each)**

Q2. Describe the thermodynamics of vapor phase growth.
Q3. What are the techniques of multilevel metallization?
Q4. Define Etching. Explain basic regimes of plasma etching.
Q5. Discuss plasma assisted deposition technique.
Q6. The yield of a VLSI chip depends on its parametric as well as functional sensitivity to the various kinds of defects, Discuss.

Section – C **(10 marks each)**

Q7. What are the various problems and concerns in Ion implantation system?
Q8. Describe the process of Silicon shaping and Wafer preparation.
Q9. Explain how VLSI assembly technologies cover the basic assembly operations for VLSI devices.