Parallax P2 Lexicon

Thanks to: Christopher Lozinski, Jon McPhalen, @EvanH and anonymous..

This document describes some l of the terms used by the P2 Community.

ADS1256: A high resolution digital to anolog converter. 24-Bit, 30kSPS, 8-Ch Delta-Sigma ADC With PGA for Factory Automation and Process Control

Breadboard; a circuit board that you can easily insert capacitors, resistors and small IC's into.

Breakout board: A breakout board exposes ("breaks-out") a circuit, function, or hardware module so it can be attached (usually temporarily) to a microprocessor. These are the "building blocks" used in early development to evaluate a design before a PCB is built.

Blinky Board: just an array of LEDs and current limiting resistors to visually show the status (on/off) of pins.

Buffered: In a hardware context, a device (gate, inverter, buffer) placed between an I/O pin and another device (often in the "outside world") to allow stiffer drive capability, waveshaping, or level conversion.

Chip: the guy who runs Parallax, and designed the chips and boards (?)

Cog: The P2 has 8 cpus each with their own memory, their own streamer, fifo, and LUTrAM and shared access to Hub resources.

Cordic: A system of math based on Logarithms. It allows for a smaller CPU than including a floating point unit.

DMA: Direct Memory Access.

DRAM: Synchronous DRAM (SDRAM) is the common form of memory used for main memory these days, Each DRAM cell is a single transistor that uses its gate capacitance to momentarily hold a charged voltage. Every cell of the array needs to be regularly (in milliseconds) read and rewritten to maintain that charge.

Dual Ported RAM. Random access memory which can be accessed simultaneously by two different circuits.

DuPont Cables:Common "jumper cables", a few inches in length, used to temporarily interconnect components/modules. "DuPont" was the company who originally made the socket/pin ends.

Edge Board. A very small board with the P2 installed. You can install the Edge board into a break out board.

EPROM: Erasable Programmable Read Only Memory: It has a window in the chip package exposing the die visually. This is used to shine UV light in and thereby erase the data, ready for programming again.

ESP8266. A very small, inexpensive circuit board with a CPU, some memory, and a wifi connection. You connect it to the P2 Eval board using the P2 Eval Adapter.

ESP32 A newer version of the ESP8266 with BlueTooth.

Evaluation Board. A circuit board with the P2 made by Parallax Inc.

FlexProp: is a simple IDE for programming the Parallax Propeller2 and/or Propeller1. It is a front end for the flexspin compiler, which can compile Spin, BASIC, PASM, or C code to Propeller 1 or 2 assembly language.

FlexSpin: is a compiler for Spin (and much of Spin2), BASIC, and C which can produce binaries for P1 and P2. FlexProp is a very simple IDE which uses flexspin.

Forth It is a stack based language, and requires very little space. Taqoz Forth is included in the Parallax P2. ze of a particularl

FTDI Manufactures the USB chips used on many Parallax boards.

Goertzel Algorithm. Calculates the size of a particular frequency component of a time based signal.

GPS Global Positioning system. Tells you where you are.

Header This is where you plug one circuit board into another one.

I2C. (Inter-Integrated Circuit) is a protocol that was developed by Philips. Used on the P1 for EEPROM memory.

IC Integrated circuit.

LFSR. Linear Feedback Shift Register. Used to generate an appearance of random numbers. The appearance is of an unchanging pre-shuffled order. Handy for procedural repetition.Random Numbers.

Loadp2: is used to load programs to the memory of a Parallax Propeller 2 ("P2") chip over a serial connection. It may also optionally execute programs from the P2 ROM (such as the built-in Forth interpreter TAQOZ) and/or send a scripted set of keystrokes to the application after loading.

LUTRAM There is Look Up Table RAM inside of each cog. This is a second block of SRAM in each of the eight Cog processors TThe reason for it being named that way is because the Streamers use it as a read-only table where it can provide colour palette register function and the like. . It is dual ported the same as the main "register" block but the ports have different use. One port is dedicated to the RDLUT/WRLUT load/store instructions of the Cog. The other port is primarily for the Cog's "Streamer" DMA engine but can also be shared with a dedicated neighbour Cog so that both see the same data in LUTRAM address space.

MQTT a Pub/Sub standard for IoT communications. Requires very low resources, and supports intermittent connections.

Nibble: 4 bits. Also called a half-byte.

P2 the nickname for the newer Parallax chip.

Palette-ing was the traditional normal solution for displaying bitmapped images with computers when DRAM sizes were constrained to a few megabytes or even less. Not used much these days though. The colour range of the display was far greater than needed to be allotted to the image being displayed. So only the needed colours were loaded into a limited set of lookup registers inside the display controller chip and the bitmap was encoded to address those lookup registers rather than with the actual colours. This allowed reducing the bitmap size from 32 bits per pixel to 8 or less. Eg: The Amiga came out with 5 bits per pixel at a time when only 2 and 3 was the norm.

Parallax Inc, the company that makes the P2.

PCB Printed circuit board

Peter Jakacki The author of Tachyon and Taqoz forth

PNut: Factory supported development tool Chip adds features and tests the compiler with his stripped-down PNut for Windows. Once these features are proven to work, Jeff moves them into the official Propeller Tool for Windows.

PROM: Programmable Read Only Memory. Also known as One-Time-Programmable (OTP).

PropLoader: is used to load programs into the memory of a P2 over Wifi. More here .

Prop Plug. A USB-to-3.3V_TTL_serial adapter -- made by Parallax for programming the P1 and the P2. If you try to program through a USb cable, every time it connects, it reboots the chip. Unless you use the Edge board with a connection that disconnects the Tx signal.

Pub/Sub Publications/Subscribe. Where some nodes on the network publish information, and others subscribe to it.

Pull Up Resistor Holds an IO pin at Vdd when that pin is floating (input state)

P2D2 a circuit board designed by Peter Jakacki

Raspberry Pi. A very low cost computer running linux.

PROM: Programable Read Only Memory.

Registers: These are the fastest type of memory. They are directly accessed by the cogs.

RS232: An EIA-specified hardware interface commonly used between "old school" computers and their terminals. Used today to communicate between microprocessors and remote devices over inexpensive cables. Generally slower than I2C and SPI, but capable of much greater distances.

SPI Serial Protocol Interface The P2 uses SPI flash for program storage.

Spin 2. The language developed by Parallax for programming the P2.

Spin2CPP: is a program for converting Spin, BASIC, or C code to binary, PASM (Parallax Propeller 1 assembly), P2ASM (Parallax P2 assembly), C, or C++.

SRAM: Static Random Access Memory. It's the fastest of the RAM types. SRAM is heavily used in microcontrollers and also for cache RAM and certain buffers in faster CPUs. Each SRAM cell is a few transistors arranged as a simplified set-reset flip-flop.

Streamer is, combined with the FIFO, a DMA like engine for pacing data to and from the I/O pins. There's one in each Cog. There is a set of instructions in the Cogs for managing their respective Streamer.

Taqoz a Forth interpreter included in 2K of ROM. Peter Jakacki's introduction.. Peter's Dropbox. Using Taqoz Forth. Taqoz glossary

TX/RX Transmit/Receive -- these are generally used as pin names for those functions. Pin 63 is programming/debugging RX, Pin 62 is programming/debugging TX on the P2

UART: Universal Asynch Receiver/Transmitter. A hardware device that handles the framing and serialization of data to be transmitted, as well as the deserialization of data as it is received.