Nov 23, 2026
Attending: Manoj, Chong, Tony, Bobae, Kirsten, Sanghoon,Dennis, Maria,

Chong -
V3 probe card
- Need another week for needle assembly company

V5 probe card
- Asked few questions to Nicolas and waiting for response

Sanghoon -
Received initial design received
    Difficult to produce extrusions
    Slightly change - but satisfy overall design and joints
- Share it through email
- AStep board populated with SMD needs to be done

Kirsten -

Toolings
- Slightly delayed
- Hopefully soon

Encapsulation
- Two trials
- One looks good
- Few wire still out
- Need to play with wirebond parameters
- Time - 10 min (need to optimize the procedure and time)
    - Get volume right
    - First step two lines on side and let it cured
    - Then do Multiple passes inbetween

Bobae -
- IV measurements

Manoj
- AstroPix v5 Delayed to December 1st shipping
- Dicing plan for v5 wafers

Maria
- Q. module status for v3 as v5 is delayed

Jinhyun/Sanghoon
- Working on Module operations (Play with firmware with v3)

Nov 16, 2026
Attending: Manoj, Chong, Dennis, Sanghoon, Blake, Kirsten, Bobae

Chong -
V3 probe
- discarded all damaged probe cards
- Producing new - needles company working on it
- Need to send it to chip test company
- They will check if it works and then Chong will visit company
- Multiple days to test multiple chips

V5 probe card design status
- Completed design document to begin design with it
- Questions to ask Nicolas
    - Studying them before sending email to Nicolas

Sanghoon
- Send the design files to company and waiting on response

Blake -
- Will reach out to company to check - delayed (follow up with company) - Oct 22 was the date
- Got quote for dummy boards
    - 5,400 for 100 of them
    - 7 weeks leadtime
- No touch option require a credit cards
    - Can Argonne do a credit card purchase
- V5 - no updates since
- Pin out, v3 astrolinx - two pins swapped - Reset vs DigInj

Kirsten -

Tooling
- All being anodised
- Will ship them this week
- Probability send them in December

Encapsulations
- Wirebonder issue
- Need to make stand posts
- No working machines

Blake (emailed)

- No AstroLinx boards yet. They had some issues and remade some. It seems to be close though.
-

Nov 9, 2026
Attending: Manoj, Chong, Jinhyun Park (Graduate Student), Sanghoon,

Jinhyun - presented 9chip pcb testbeam and injection studies

Chong -

Nov 2, 2026
Attending: Manoj, Chong, Tony, Bobae

Yonsei
V3 Probe card repair Nov 11-12
Send it to Chip test machine company
Once they align - then Chong will visit company
They have more v3 chips after dicing wafer
Realistic mass Q/A using these chips

V5 probe card
Gathering all information and giving it to expert

UCSC
will get tooling in a week or so

Oct 26, 2026
Attending: Manoj, Chong, Tony, Kirsten, Sanghoon, Blake, Dennis

Probe Card /Chip QC
- Visited company
- Forwarded the material to engineers
- Discussed producing probecard
- Chip carrier from 9-chip pcb - If can make it to end of this year
- Data rate issue - loss of data package
    - After discussion
        - Understand v5 chip and then design probe card
    - Backup
        - Continue design with GECCO board
    - Updating v3 probe cards, checking mechanical touchdown needs to be checked

    - After that we can check v5 probe card
- Not sure when we will receive repairing probe cards

- Chip Framework: not sure develop further with v3
- New date for AstroPix v5 shipping - 12 Nov 2026

UCSC
Glue trials last week
Made some wedges - sample pieces at 15 deg angle etc. not good coverage
Tooling - finishing machining to end of this week, put together 2-3 weeks
Other Tech - put together DAQ

Oct 14, 2026
Attending: Manoj, Chong, Dan, Sanghoon, Adrien,

Strategy discussion for AstroPix v5 probe card

V5 chip probecard design
Wafer will be delivered end of October
Mass chip A/QC starts mid December
Idea is instead of using GECCO+Nexys -> use AStep hardware

Plan is to go forward with AStep hardware and later if needed we can upgrade it to compatible FPGA from ETC card

Data rate needs to be checked 1Mbit/sec is limit for cmod 7
Adrien calculated on the fly rate for all pixel injections with 14 bit per hit -> more like 1 Mbit / sec so at limit -> might not be the issue

Oct 12, 2026
Attending: Manoj, Chong, Tony, Sanghoon,

Yonsei University -
Chong -
- Probe card - 2 options
    - Similar to current design (GECCO-Nexys)
    - Ask Engineer to build new probe card compatible with AStep FW/SW
        - Complex but if we can do it that would be compatible with AStep SW which will be used to test modules
        - Robustness of readout chain

        - We decided to go with new probecard design using NASA AStep CMOD FPGA
        - Two test article -> for bare chip and single chip carrier board
- Sent broken v3 probe cards to company - two probe cards completely damaged -> all needles needs to be replaced with new -> will take time to get that work done
- Once I receive them will send it to chip testing company
- During repair -> they will add some alignment marks on probe card

USCS
- P.O. went in for tooling

Argonne
- Started characterizing chips for module assembly
- Looking into inventory to send chips to different sites

Oct 05, 2026
Attending: Manoj, Chong, Blake, Tony, Kirsten, Bobae

Yonsei University -
Chong - alignment without markers is still going on
- Read the email for the v5 probe card
- Sent an email to the probe card designer with the v5 chip design and electrical schematic with a single chip carrier board
- Which direction should the v5 probe card move - Chong and Shanghoon
- If the probe designer designs the probe card, then it would be custom firmware.
- V5 probecard will be ideal if it is compatible with AStep
- Send damaged probe cards this week and expect to get them back faster

Oklahoma State University -
- No news about Astrolinx
- Dummy board - made progress, but will know more tomorrow about the status
- V5 - met with chip designers last week
    - Got a lot of information about the pinout
    - https://docs.google.com/spreadsheets/d/1w3gPzJTv5pHb9EoUAYuOapxyBJsiOj_nnp0lAQ7FitE/edit?gid=1520044715#gid=1520044715
    - Started with a new iteration
    - Current stack up is just under 1.2 mm
    - Did bunch of simulation to find another stackup which might be similar
    - Found few similar - probably be more ideal for space we have
    - Little more extra design as we need to reduce layers or 300 micron tracks with current
    - With 0.8 stack the track width will be half.
    - Impedance drops to 20-30 if you have a bigger pad (300 um) with a trace of 150 um.
    - Wirebond current limit is 3/10s of amps ?? get a data
    - What Noise level on the power regulator ??

UCSC -

- Glue trials with Dymex
- 3 trials
- No time to work on the stencil
- Manoj to send the instructions on the workbench

Sep 29, 2026
Discussion about v5 pin-out for BIC modules and AstroLinx readout

Attending: Manoj, Dan, Adam, Adrien, Nicolas, Blake, Steven, Evan Cole, Chong,

Can be narrowed down to 1 LDO per board

Good filtering between analog (vdda and vssa) and digital

Current values are preliminary numbers (will be updated)

LVDS receivers and drivers

In v5 there is also SPI left interface - there is a differential pads on bottom so basically you can also connect to first chip of chain differentially and so these are the specification of on-chip drivers on MISO lines

Specs for receivers for miso and clk and chipsel

If you don't use diff spi then you dont need it

Also possibility to supply external timestamp clock exetenally but guess it might not be uses

Syncres - resets internal timestamp counter

SPI lines diff vs single ended

NIcolas - if you have very long traces and spi interface catchup lot of noise then you need differential

The problem with single ended SPI might also be reflections at 2m length and 20 MHz.

Steven - length for SPI reliability is around 10 m before you need to worry

Do all of the pads for low voltages need to be connected??

- Adam - for ComPair skipping a bunch
- Nicolas - total current is a few mA, so it is fine to connect a few wirebonds
    - They are all connected internally to same power grid

Grounds can also be reduces, keep enough for the digital and analog part

HitBus - can be used as output trigger and can be used for synchronization

Digital inj - also have internal pulse generator

Sep 28, 2026
Attending: Manoj, Chong, Bobae, Kirsten, Tony

Yonsei
For v5 and v6 - There will be no alignment marks for chip testing
Alignment markers for the ALPIDE chip were sent to Nicolas

What shape do they need? - Tony
Shanghoon -
Need to check with the company, but cross-mark with a few microns
Other shapes that they need will be discussed today

Tony -
Some machines need a round shape, some need something else
Depends on the algorithm

Postprocessing - might not be a good idea
But for the next round of 85 wafers, we can go for it to implement in the fabrication process

Nicolas - it is Euro10k for two additional masks (email)

Discuss with engineers today.

UCSC
Order went in for toolings
Ready in about a month

Send DAQ information to UCSC
Testing setup back on track

OSU
AstroLinx - PO out and got the confirmation that the rigid boards are in fabrication
Testing AstroLinx flexes, 6 or 8 are tested (3 of each for each site)
Yes
Dummy Rigid - 3 weeks from now to get it (if we finish it)
Need it for mechanical stuff
Don’t think it hurt (Tony)

Sep 21, 2026
Attending: Manoj, Chong, Blake,

Sep 14, 2026
Attending: Manoj, Chong, Blake, Tony, Kirsten

Aug 24, 2026
Attending: Manoj, Chong, Kirsten, Blake,

UCSC
Did tests for possible glues for encapsulation
Dummy PCB to half moon Al from ATLAS

Options tried
Sylgard 186 - mixing, 24 cure time
ResinLab UR3010 - very thin - runs down very easily - cure time 24 hours
Dymax UV - medium, cures in 5 min, no mixing - easy

Need to test
Stycast 2850

Bld is closed for 2 weeks from now

After coming back, write a program to do the encapsulation

Tooling - have not heard from the tooling vendor, have a second option
Stencil for HV check - will work on it this week

Oklahoma State - Not much updates
Not started on testing of flexes - soon
Trying to get started on dummy board - priority

AstroLinx order still at Oklahoma State - will get in touch with admin
Blake - traveling for the next two weeks (ITk week)

Yonsei -
Chip test machine company - Early September
Sanghoon is at CERN for the testbeam
Will contact probe card company this week about v5

Aug 17, 2026
Attending: Manoj, Chong, Tony, Kirsten, Blake,

Chong

Contacting the chip testing company

- Delayed
- Early september
    - Does the entire communication work?
    - Probe card alignment
    - Establish communication between chip and DAQ
- On-site test at the end of this month
- For v5 probe card - need carrier design

Blake -

Going through approval
PO end of the week
20 days lead time

Also, dummy PCB - need it in 1-2 weeks in hand so can do mock-ups

Engineering meeting at NASA - Nov first week

Kirsten

- Updated AstroLinx PCB and chip pad don’t match
- Blake shared Altium project with Kiesten and Tony so they can access the net names for pads
- Made Samples to play with encapsulant this weeks plan
-

Aug 10, 2026
Attending: Manoj, Chong, Tony, Sanghoon

Setting up the test bench at Yonsei
Same company to discuss module assembly
Sent the Al 3D design for extrusion with cutting method (couple of weeks to produce initial samples and try to do dummy module assembly with pick-n-place machine)
Related presentation - around next week (glue, encapsulation)

Forest put some test structures together for assembly
Kirsten is writing a program and has everything ready with encapsulation samples
6-8 weeks turnaround for toolings

Aug 3, 2026
Attending: Manoj, Chong, Blake, Steven, Sanghoon,

1. Adapter Card and QA Testing
High-noise issue with the adapter-card setup was investigated.

Additional debugging showed that the adapter card is not the main source of the large noise.
The 2.7 V supply to the GECCO board must be provided correctly.
Preliminary QA tests will check:
Electrical contact between the probe-card and bare chip
Communication/functionality
IV and related scans
Lab setup will be completed this week, with on-site testing targeted for mid/late August.

2. V5 Pro-Card Development
V5 preparation should proceed in parallel to avoid delays.
Preferred design is a single-form-factor probe-card integrating the required functions.
The team will discuss the detailed V5 design and testing requirements offline.

3. AstroLinx
BOM was corrected and obsolete components replaced.
Updated BOM was sent for quotation; vendor response expected by mid-week.
Wire-bond practice boards will be fabricated, likely through a quick-turn vendor.

4. Production Reporting
Each site will provide monthly progress against its SOW.
Percentage completion will be estimated based on milestones and completed work.
Reporting will be discussed further during the monthly meeting.

5. Chip Modules and Beam Test
Nine modules were assembled but are currently not functioning correctly.
One additional card/chip assembly will be evaluated and potentially corrected.
Future beam-test planning is underway for approximately November–December, including multiple chip-PCBs and DAQ integration.

July 27, 2026
Attending: Manoj, Blake, Adam, Maria, Bobae, Chong, Sanghoon

July 20, 2026
Attending: Manoj, Tony, Blake, Bobae, Chong

July 14, 2026
Attending: Manoj, Kirsten, Tony, Sanghoon

July 6, 2026
Attending: Manoj, Chong, Kirsten, Bobae, Tony, Sanghoon, Woojun Park, Kookhyun Kang

Schedule update
Sanghoon - Module assembly machines

PNU -

Chong -
Tried to do some field tests with the test company
Chain of system works?

- Gecco board, fpga, new probe card, adaptor card
- Suspicion about adaptor card produces large noise
- Progress studies to identify the issue
- Discussion with the expert who created this adaptor card.
- Tuning or repair - next two weeks
    - Send Chong link to upload schematic for adaptor card

Sanghoon -
Module Assembly in Korea (Not for EIC)

- Outer tracker ALICE3 experiment
- Chip placement - is there vacuum for each chip? (Tony) - Same line but with small holes
- Is vacuum on while put the chip on or after (Tony)
    - While we put the chip on, need to check
- Heat cure epoxy is used (1125) - see some mis alignment after curing
- Die bonder machine has glue dispenser
- For BIC can produce customised machine to do similar work (C-ON tech)
- C-ON tech is the company which will do chip testing
- Will start customized module assembly
- Glue 353ND
    - UCSC uses something similar
    - What kind of coverage? Not a lot success getting coverage
    - Does it need a heat cure?
        - RT for 24 hours
- Use machine chip to locate
    - Where chips are placed?
    - Carbon fiber tray / gel pack
    - Used for ITS2
- Need some information slides about how to pack ship chips
    - In couple weeks
- Slide 13
    - How do you align chip and pcb jig
    - Chip are floating on pcb for 24 hours and still seen aligned
- One big machine have full chain but also need to catch up with throughput of chips

UCSC
Kirsten

- Nordson
    - Have 2 robots
    - By the time of BIC production this should be available
    - How to use 2 component epoxy
    - There is a bracket to hold two component cartridge holder
    - 3k USD
    - For encapsulation
        - Dymax - uv cure

        - Stycast - catalyst (several)
    -

June 29, 2026
Attending: Manoj, Bobae, Tony,

Summary update from BIC workshop

Quote for tooling expected next week
Glue mixing using Nordon glue robot - discussing it with Nordon rep for solution to mix two part epoxy on the machine

June 1, 2026
Attending: Manoj, Chong, Tony,

Chong -
    Adaptor card is completed
    The new probe card should include everything
    5V converts to 1.2V and 1.8V
    AStep firmware and software

March 30, 2026
Attending: Manoj, Chong, Tony, Kirsten, Sanghoon

PNU
- Adaptor card expected to be delivered by May 20th
- Late May to test the card
- Probe cards - 3, adaptor cards - 2 or more.
- At NOTICE and then on site

    QA framework
    - github repo
    - Upgrade to v5
    - Use A-STEP firmware
    - Currently, the setup of the FPGA is provided by an external power supply - no IV scan can be done.

UCSC
-

March 30, 2026
Attending: Manoj, Chong, Tony, Kirsten

PNU
- Adaptor card promised to be delivered by May 20?
- Can prepare some software to test the card
- Busy with testbeam, but QA is still going on
- DAQ is in Python, but analysis is in C++
- Interface between these two to get the final results
- Present details of QA/QC next week

ANL
- Will ship dummy chips to UCSC
- Shipped FPGA(2), and 9chip PCB and cable to Sanghoon
- Tasks for Manoj
    - Extrusion follow-up (ANL order)?
    - Get the reviewers' comments on Toolings
    - Check with OSU about AstroLinx/Readout boards

April 13, 2026 - Assembly Tooling Review and general meeting
Attending: Kirsten, Tony, Jessica, Forest, Kevin, Tim, Manoj, Sanghoon, Chong,

The gap between chips, 100 microns, is too hard
- Increasing the gap will make things easier

Kevin
- machine shop - company makes tooling for silicon carbide
- Made prototyping
- Tolerances are too tight - can they make it?

PNU
- Adaptor card - working on circuitry - finishing this week. Will check with him
- Fabrication is faster - it is already prepared in the company process - 1 week or 2

- Software - progress about software test routine
    - Chip can communicate with the software
        - Take the file, injection, and threshold
        - Need to add more routine
        - AStep FW/SW

April 06, 2026
Attending: Manoj, Tony

USCS -

For a chip pick-up tool

Working on another option instead of screws/pins to hold them together
Maybe magnetic posts
Printing a few test articles with the new design
Review next week, okay

ANL

Kevin moved forward with Al base plate order
Lead time delivery June 2026

March 30, 2026
Attending: Manoj, Chong, Tony, Kevin, Sanghoon

PNU

- Adaptor card is being developed.
- Meeting tomorrow with the engineer
- Will test in the lab without a full setup
- Testing using the AStep - DAQ chain is working
    - Script and injection working is tested
    - If this test can be tested using a bare chip

UCSC

- 3D printed parts
- Aluminum extrusion doesn't fit
- Review in 2 weeks
- Encapsulation
    - Start discussion
    - Write down the requirements
    - In the assembly procedure
    - Dedicated discussion

March 23, 2026
Attending: Manoj, Chong, Sanghoon, Kevin

PNU

- Probe card adaptor - the engineer started work
    - discussed a few things
    - Found a bug with the current version
    - Power issues - can not be tested
    - Test signal pins one by one
- Trouble with AStep SW/FW
    - AStep software is not very well prepared at the moment
    - Can't use it directly for this task
    - Can make some progress this week
    - If it still gives issues, then roll back to Python-based scripts

ANL

- Meet with Kevin and Tim to go over the design files of tooling and basically what we want to achieve with these toolings

March 16, 2026

Attending: Manoj, Tony, Kirsten, Sanghoon, Adam, Bobae

UCSC -
3D printed everything
Will 3D print a hybrid with PLA to play with it
Still need a solution for the chip location
Next week at CERN for ITkWeek
Extrusion to UCSC and dummy modules.

PNU -
Working on the AStep testing setup
The probe card touch-down adaptor is going back and forth.

ANL -
No updates

March 9, 2026 (Cancelled)

Attending: Manoj

Cancelling the meeting

March 2, 2026

Attending: Tony, Manoj, Bobae, Sanghoon

ANL

- Testing the external clock with the latest bit files
- Preparing for the March Hall D beam test

UCSC

- 3D printed toolings are delivered
- Hybrid pick-up
- Chip pickup
- What do we need to go into the review for toolings
- Organise a meeting on glue (robot, working glue life) and encapsulation (is it possible?)? - understand what constraints are

PNU

- No particular news
- Chong continued testing the chip for Chip QC - successfully tested using AStep FW/SW
- Sent 9-chip PCB boards

Feb 23, 2026

Attending: Chong, Bobae, Manoj, Kevin, Tony, Kirsten

UCSC

- Wirebond test on Extrusion
- Glass and dummy chips - works well
- Pull tests were good (~9-10 gms)
- PCB to chip wire bonding

- Encapsulation - not obvious
- Decision on the glue

- Toolings
    - **Dedicated review for Toolings**
    - 3D printed tools for Review
    - 3 copies single set by in-person meeting (June 16-18)

PNU

- Contacting probe card engineer - no promises, but will work on it

ANL

- Testing module PCB, preparing for test beam
- Received AStep FPGA boards - 5 (two will go to PNU, 3 are available)
- AStroPix v5 fabrication began at AMS (making masks), another foundry option, LFoundry - 2 x 3 cm2 reticle size possible

Feb 16, 2026

Attending: Chong, Manoj, Kevin

PNU

- Holiday
- Plan to continue testing
- Probe adaptor card - engineer - still haven't started working on it
- How the V5 architect is designed (hit buffer for each pixel)
    - How signal sent to the digital periphery
    - Any chances of a pile-up for multi-pixel injections
- AStep firmware - discussion

Feb 11, 2026
DAQ-Module joint meeting

Attending: Chong, Halen Davies, Akshaya, Beattite, Regina, Adam, Blake, Manoj, Adrien, Aram, Dan, Shefali, Shinhyungkim, Zisis, Maria,

Introduction to modules - Manoj
- 9 AstroPix chips on module
- 12 modules on Stave
- 6 - 7 Stave on a tray
- 2 trays per sector layer

Introduction to AstroLinx - Blake
- question - Driven, source series termination (Adam) For signal runs through cables that are not daisy-chained
  - Signal loss at the end of the chain
  - There are some termination resistors

ComPair2 FEE -
- Shown at AstroPix workshop
- Lattice CErtusPro
- DC-DC converters for housekeeping
- 20-pin connector with 20 lanes
- DC to DC screenshot
- Lanes with a bus

ComPair2 is switching to the Lattice non-pro version, so downgrading to use free licensing for flashing the FPGA

How we would like to approach EPIC design is to take this design or take a smaller version of the FPGA
Match the new form factor.

12 cm to 16 cm trapezoid for the ETC card

Adam -
- Can do a lot of options on PPT
- But need dxf from the mechanical engineer

Time slot
- End-of-sector box meeting at 8 am
- But we can set up a doodle poll for the new slot.
- Figure out the slot.

Feb 9, 2026
Attending: Manoj, Chong, Bobae, Sanghoon, Tony, Kirsten,

PNU

Probe card chip testing procedure

Tentative plan in four parts

Initialize - FW/SW configuration, touch down, power up

Test -

Analysis

Cleanup

ALICE ALPIDE - also upload the results to the database - provide a summary report

Initial test items and injection studies

Initial test items

- **Initial test items plan to implement**
  - Communication check and Register R/W
    a. Board ↔ chip communication (to check if the chip is alive)
    b. Register map check: key register values write/readback
    c. Record: bias voltage, current, temperature, fw, entire register map
  - Basic performance: require parameters study and tune
    a. Noise scan: # of hot/dead pixels, generate occupancy map
    b. Injection scan: by using low and stable event rate
    c. Threshold scan: generate s-curves for multiple points
    d. Record: results plots generated by ROOT
  - Stability
    a. Generate 2D hit map in "standard" setup (e.g., bias -200V, threshold 200 mV, runtime 30s, etc)
    b. Repeat at least 3 times and check consistency
    c. Record: hit maps

Injection studies

Single pixel

Single row or col

All rows and cols

Injection study (2/3)

- **Rate capability of single pixel (c10, r10)**
  - Official info vs. Measurement
    a. Spec: 4 Hz/pixel (arXiv:2511.05639)
    → This limit seems like operational condition, rather than the physical/technical one
    b. Parameters relevant to event rate being injected (astropix-python):
    b-1. Inj_period (0, 255)
    b-2. clkdiv (1, 65535): default 300
    b-3. Judging from data, $f_{inj} = \frac{f_{sysclk}}{256 \cdot clkdiv \cdot (inj_period + 1)}$, f_{sysclk} = 100 MHz, given by Nexys-video
    c. Conditions: single pixel injection (c10, r10), -150V (bias), 400 mV (threshold), 500 mV (inj_voltage), 10 s (runtime)
    d. Repeated same measurements for 3 different chips (w102s08, s10, s12): consistent

inj_period	clkdiv	n_lines	n_readout	File size (kB) (* csv decoded)	Contamination	Rate (Hz)
0	300	65,144	1,666	3,742	?	?
10		2,495	1,247	141	N	~125
100		259	239	15	N	~13
162		159	79	9	N	8.0
255		101	50	6	N	5.1

Injection study (3/3)

- **Rate capability of all pixels**
  - Scanned inj_period and clkdiv
    a. Data starting to be contaminated (truncated packet, corrupted row/col consistency, readout overlap, etc.), if the inj_period is lower than 162 (event rate is higher than 8.0 Hz)
    b. For chip performance test purpose,
    b-1. 7 ~ 7.5 Hz injection rate
    b-2. A few tenth seconds of runtime
    c. If necessary, clkdiv can be utilized for extremely high/slow event rate
    d. Tentative test procedure: default (7 Hz + 30s) + precision (only when the status looks suspicious)

inj_period	clkdiv	n_lines	n_readout	File size (kB) (* csv decoded)	Contamination	Rate (Hz)
100	300	9,096	259	498	Y (substantial)	~13
129		7,065	201	386	Y (substantial)	~10
162		5,682	161	310	Y (slightly)	8.0
255		3,885	114	210	N	5.1
	600	1,821	52	98	? (not checked)	2.6
	150	7,141	205	389	? (not checked)	10.1

LAST SLIDE

ANL

9 chip updates

First module #4 works with chip 8 gives 0 ToT

Two more modules, 7 and 8 working after the correction to PCB - chip 2, 5, and 8 don't work

Plan for testbeam

10MHz with private code

40MHz needs to be checked

Need longer cables between SFILs

Feb 2, 2026

Attending: Manoj, Chong, Bobae, Kevin, Blake, Jinhyun

PNU

- Jinhyun joined the PNU team (graduate student)
- Probe card to perform chip test
  - No progress
  - Contact the electronics company to get the status
  - Waiting for a reply
  - Preparing the electrical contact routine - end of this month, Feb (but busy person)
  - Regina and other members want to touch base with the Astep firmware to use a common decoder
  - Performed actual routine to perform the injection with astropix-python - inj for the whole row/col - this week's plan
- Sanghoon
  - Will send AStep FPGA boards next week
  - Will fabricate a base plate with a sharp corner to test assembly precision
  - Let Manoj know if round corner base plates are needed to do additional tests
  - Meeting with the company next week

Oklahoma

- SoW - finance person helping with BNL to get it out sooner
- Placed all the orders
  - But they don’t want to pay the PO until they get approval
  - Start getting boards in a couple of weeks

ANL

- Testing the quadchip and 9-chip PCB board
- Beam test at Hall D in March (10th?)
- A Step board and a quad chip
- Comparison with the previous KEK beam test
- Have a readout rate limit and a count rate limitation
- Long-term FY26
  - AstroPix with ETC
- One 9-chip module is working
  - One more under debugging
  - Tried to test module 7 and saw some solder detached, and need to check
- Send Schematic file link to Blake to look into HV biasing issue

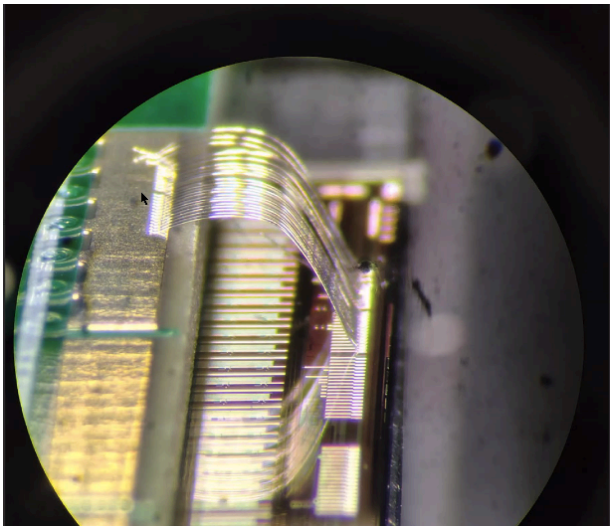
Jan 5, 2026
Attending: Manoj, Chong, Bobae, Kevin, Jessica, Sanghoon, Tony,

PNU

- Adaptor card starts end of January and is delivered at the end of February
    - Fabrication is very straightforward
- Sanghoon needs a “working file” for the automated population of PCB
- Dummy chips this week (300)

UCSC

- Kirsten was working on drawing - 3D printing - half of them done - adjusting the other two
- Bonding trials - good bonding
    - 9 gm



Wirebond from bottom to top or otherwise -> top to bottom (more common practice)

Stencil to adjust spaces between chips
Movement of chips - holding the chip down
Fix the glue
Try a couple of things and see what happens

ANL -
Bobae

- AstroPix chip testing
- 3 quadchip working well
- V4 chip not responding to injections
- Hgc3roc for synchronisation
- Two more 9-chip boards need to be debugged

Jan 5, 2026
Attending: Manoj, Bobae, Chong, Tony, Sanghoon, Kirsten,

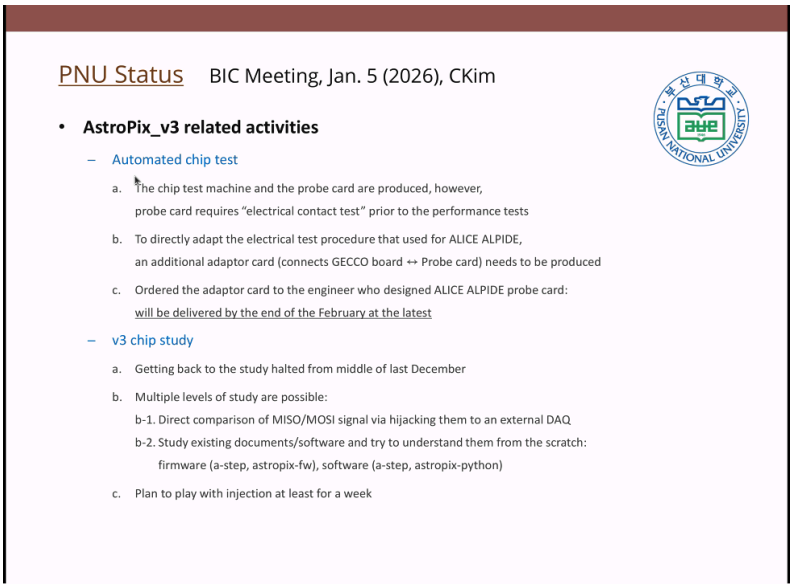
Workfest -

workfest for wafers and modules for BIC imaging layers.
Discussion about AstroLinx and ETC with people from NASA and Oklahoma State.
Wednesday afternoon?

Tooling and wire bond challenges with module-based design
Mitigation to achieve a 100-micron gap between chips
Keeping the option to have a pick-n-place machine for assembly as a backup plan

There is someone from UCSC coming, and we will be discussing tooling with them. If either or both of you can come, we can plan something to discuss the interface between AstroLinx and ETC with NASA people, and I can see if they can come.

PNU -



End of February - the adaptor card will be delivered to PNU

Data waveform structure for chip testing firmware

Sanghoon -
A Step hardware PCB

- started to get quotes
- Buy the components (difficult to make big contracts)
- Start with 5 before Feb

- The new fiscal year starts in March - then do the remaining

Dummy chips
    Start sending them
Bobae -

UCSC -

Send Kirsten updated drawings

3D hybrid tools
    3D print samples of them -
    https://anl.box.com/s/g9zgrrjtgq3ll050u2tk8yabt4w4yquo

    All the drawings are consistent with the center of the Al plate

Dec 15, 2025
Attending: Manoj, Kevin, Tony, Chong,

Workfest during ePIC meeting -
    Email with details to Tony+

Kevin -
    Drawings with the latest AstroLinx board and fitting in the envelope
    Include glue layers
    Latest AstroLinx PCB
    Centered on Module
    0.2 mm lost in reverse flipping
    Connector flex PCB is 13mm -> can be smaller

    Vendor for extrusions - nice job - in specs and tolerance
        Current Tray with one wide piece
            The lightest piece can be smaller than 4 inches
            Two-piece Trays
            One more thing to do before attaching them
            Bond them permanently and handle them as a single piece

UCSC -

PNU - Chong

- Probe card - contacted design engineer
- The engineer confirmed that he will start working on the design
- Adaptor card touch-down method
    - Electrical contact procedure to start testing

        - Fastest expected time middle of January next year
- Resumed testing on the v3 chip
    - A few questions - raised during the AstroPix meeting
    - Resume the study after Christmas
- Probe is under testing
    - Assembly completed - 3
    - Sent to the chip testing company
        - Connect it to the machine and test it
        - The chip testing company is waiting for the electrical contact procedure

Dec 8, 2025
Attending: Manoj, Chong,

Nov 24, 2025

Attending: Manoj, Chong, Bobae,

3 probe cards fabricated - expected early next week (end of this month)
Write to Nicolas and Richard to have a meeting for the Probe card discussion

Not gonna take

Nov 10, 2025

Attending: Manoj, Chong, Bobae, Blake, Tony, Maria

OkState -
Quantity 30 - 10k
With the other 2 items - 16k total
Is it for everything, fabrication, and population? - It is the fabrication and assembly of a rigid board - 10k
40-pin to 60-pin

AstroLinx PCB is designed
Procurement process started for AstroLinx Regid board
Final changes for flex and readout board
    Set up the review when that is done
Order placed before the contract ends for current funding
Some QA/QC test stand options are a little bit different from what we are used to
    Because of the wirebond pads

What is the stack?
    1.2 mm pcb + 2 mm connector + 0.3 mm (0.5 mm stiffner)

Greg sent out CADs to Kevin and Ron to check if they fit the envelope (maybe he didn't).

PNU -
Probe Card - is with the needle assembly company - by the end of this month
Preparing software - Python software is going slowly
DAQ and decoder with C++
Received the AStep FPGA PCB and will take a look at it this week.

Email about dummy chip - produced
10 6' 6-inch wafers are produced and diced.
Dummy module assembly - Al with the company, and check the quality and procedure.
Please send us 6 wafers with dummy chips.

Argonne -
Had a meeting with the Representatives from the Aluminum extrusion company.
Kevin, Tom, and Ron joined
I was there for a brief discussion in the initial 30 minutes
They can not do 0.5mm thin flat edges of the module
They can do a slanted edge and a 1 mm flat edge
They can only do ~4cm wide single-piece extrusion

Proposal-
One-day or half-day workshop - either in-person or remote
Brainstorming all the technical details of the modules and the envelope
Assembly procedures, numbers, etc.
Options for production

UCSC -

We can try to do a tapered edge, and Forest can try to see
Kirsten can design a tapered edge
Try to design with a tapered edge

Final drawing for both - Ron and Kevin send the final drawings of both designs of Staves

Did not get a chance to do the cantilever test - wirebond

Nov 10, 2025
Modules and Wafers

Attending: Manoj, Chong, Tony, Bobae,

Agenda for this week -
News from the project side, summary of the joint meeting between Modules and Mechanics
Update on AstroLinx PCB, Readout board, and Flex Jumper
Update on assembly toolings (note - we are waiting on the extrusion profile from mechanics)
AstroPix chip testing stand and probe card

Chong - Sanghoon is in Conference - organizer for conference in S.Korea - so may not join

Wafer -
PNU -
Chong - Still ongoing, probe card and chip testing system
    Probe card PCB is produced
    Some of the components arrive internationally, so expect some delay
        End of this month to early December
        AstroPix Python and FW package
        Software - stably run and extract data with existing code
        SPI protocol - make sure
No status about - AStep FPGA PCB
    Holding at the Customs

UCSC -
Need a conversation about additional space - it is too constrained
Did not follow up on Forest -
    Check with in in-hand AI plate and AstroPix
        Share AstroPix v3 with 500 um bad chips - will send it to UCSC

Plan a module meeting, brainstorming!
    Might invite someone who uses a pick and place machine for strips
        One of the Canadian group, or Oxford group, or the Purdue group
        Visit the site to learn - before meeting Mathew Jones (Purdue)

ANL -
9chip testing - no slides
    Reworking with Sr90 data taking with different time 5sec, 15sec up to 1 hour
    Data rate and hits per pixel
    1k event per pixel, around 1 hour
Running 3 quad-chip -
    Quadhcip masking
    The new Quadchip didn't work for chips 2 and 3.
    Wire-bonding needs to be checked.

Nov 5, 2025
Joint meeting Modules and Mechanics

Attending: Blake, Tony, Forest, rtkmak, Kevin, Vic, Sylvester, Tom, Manoj, Kirsten,

Old profile has a flat edge -
New profile has wings
- Need flat support and also an edge to align the modules
- The corner at the edge doesn't allow for to placement of the base plate flat
- Another difficulty is that we now have a very small area to put vacuum holes in the middle
    - Chip could rock while assembling
    - Even with tight channels
- Wirebonding

    - Bonding at the edge of the extrusion
        - So not ideal for flat support
- Sylvester
    - This needs to be placed close
    - How hard can the corner be extruded
    - Hard to extrude if it is too thin

Extrusion company in town next Friday - will talk with them and get more information
14th - get profile information
Not meeting before that
Can also reach out to the company and talk to them

Circuit thickness: When to obtain information?

Try to negotiate 0.5 cm space inside of detector - Al plate
Need to talk to the project.

3.5 mm => 1.2 rigid + 2 mm connector + 0.3 mm

Oct 27, 2025
Attending: Forest, Manoj, Tony, Kirsten, Kevin, Blake,

Agenda -
Tooling updates
Astrolinx progress
9chip PCB testing

PNU
The dummy chip has been prepared,
How many chips are needed for the assembly test?
All wafers are diced, so I can send them after detaching the diced chips from the tapes.

Argonne

OkState
Blake - haven't had a chance to talk to Greg today
The rigid portion is pretty close to done

Flex is being designed
Connector is changed - a lot of the same thing with a longer length, Same height
Stack up a 1.1952 +/- 0.1 mm thick rigid portion
The flex region should be around <0.3 mm
Kirsten -> What is the height of the PCB -> 1.1952 +/- 0.1 mm
Blake -> alignment pins - will check? How much does it stick out from the back of the flex
No alignment pins on the Rigid part of the AstroLinx
Right now, we have a lot of power planes -> if it is too much copper (testing through pre-production), the option may be to get rid of copper for power is one option in the future

UCSC

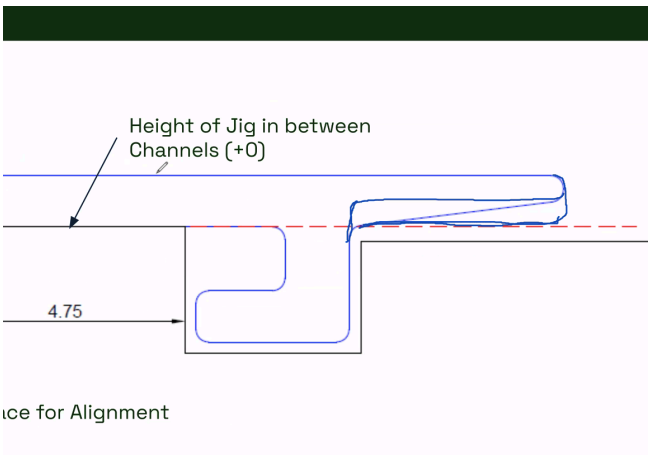
Metaphor: Aluminum for the vacuum - chip pickup tool for now
Misumi alignment pins - diamond and round edge mixup

Chip pickup tool drawings are pretty much done
The chip alignment tool is challenging
1.3 mm gap for v3 and v5
Stencil tools

Chip Aligner
Option 1
Stencil - challenging for v6, 100 um
Option 2
Vertical slot
Require hand-crafting

Hybrid Pickup tool
2 vacuum pins for the connector side and 3 more along the length
Need connector part number (Blake will provide it)

The extrusion profile was wrong
Concerns with the new design
Edges are at an angle
- So they can tilt while assembly
- Also issue with wirebonding



-
- Blake - slide 6, tolerance for PCB can cause any tolerance
- Write to Sylvester and Mechanics
- Get input from the Stecil company

PNU

Dummy chips are ready to be shipped

AstroPix probe card is ready

PCB is ready in two weeks from now

AStep FW/SW run with single chips

I can take the data only once

Have to restart the system

The chip test machine is now being produced and is under calibration and tuning stage - dummy probe card for other chips

Having a meeting weekly

Tony is up

Blake - late time slot is difficult

Sep 29, 2025

Attending: Chong, Blake, Tony, Sanghoon, Manoj, Kevin

OSU

Paused the order

Greg started working on the design - a two-piece module

PCB + jumper cable

Go ahead and switch to the final connector

Put enough pins and route enough traces to connect 12 modules

Chip select and interrupt for 12 modules (vs. 6 modules)

Take out some of the power scheme

Placement of the chips - need a drawing (Kirsten's PPT?)

End-of-Tray Card - haven’t started yet, so change of connector will not yet affect ETC design

UCSC

100 micron is difficult
We can't progress the v3 version stuff

Very near future - need to get this done

PNU

Dummy sensors under production
    Not able to change the pads
    Fabrication of 10 wafers 6 inches are under fabrication
We can use the first production results as a trial for assembly, and after checking the status, we can proceed with the second batch.

ANL

FPGA boards are fabricated, waiting for population
Will send them to PNU
Along with that, we will send one 9-chip PCB - unpopulated
    Snaghoon will try assembly and test
    If it doesn't work, Argonne will send him a working 9-chip PCB
9chip PCB setup move to cleanroom - Bobae
    Will start testing other boards now.

Sep 15, 2025
Attending: Chong, Bobae, Maria, Blake, Tony, Sanghoon, Manoj

PNU
Probe card is almost finalized - final confirmation from the company
    One try, and if everything works fine
        Update later
    Started looking around the firmware system
        PNU (Yoonha) tested single chip (v3)
        No problem so far wrt FW/SW
        Plan to write a compatible version with v3 to take data
        All chips are v3 at PNU
            Can we run FW/SW?
QC test setup - Sanghoon is travelling - sometimes this or next week, ready to test
    Probe card ready - need to check leadtime (end of this month)

OSU
We are pushing the order through the bridge card
    Module PCB - ON hold (what is the new plan?)
    Focusing on Review
    Blake at CERN next two weeks

UCSC

Three stencils
    Can’t use it for anything
    Can do v3 chips
NCE got through today
Kirsten's computer is back with powerful CAD
Working on Hybrid details - placement pickup tools

Longer terms v5 - need to discuss
One stencil with different widths of bars

Very thin stencil, so try out different thicknesses
4 weeks from now, we will go over stencil, pickup tool designs
    Oct 13th

ANL
9chip PCB testing done with v3

Dry Run - Bobae

Dry Run - Greg

Aug 4, 2025
Attending: Chong, Blake, Bobae, Forest, Manoj, Yoonha, Tony, Kirsten, Kevin

1. AstroLinx PCB design signup
    Finished the design over the weekend
    Few more things to correct - suggestion from Blake
    Ground pad extension is still pending
    A week and a half to get it on the floor for fabrication
2. AstroPix dummy chip fabrication
    Chong - dummy chip fabrication - email exchange
        They requested the final dimension for submission for 10-20 units

3. 9Chip PCB board testing updates
    9chip pcb injections
    Issues
        Lower analog output
        No injections at the periphery
        Max buffer output

Tony (new design Review comments)
    Page 4 Layer 6 copper is missing in some areas (Layer 7)
    Small cleanup

4. Assembly tooling updates
    Have ordered glass chips with v3 v5
    Ordered alignment stencils to place the chips on the extrusions
    250 µm to xxx gap
    Chip aligned to the bottom left corner of the 20 x 20 pocket

Announcement:
    PDR on Sep 17 and 18
    Couple talks from Modules and wafers
        Modules/Staves
        AstroLinx
        9chip PCB testing (combined with System Testing)

Jul 21, 2025

AstroLinx Internal Review -

Attending: Tim, Steven, Tony, Manoj, Regina, Adrien, Kevin, Blake, Jessica, Maria, Dan, Chong, Bobae

Aligned with the left edge
Thinner wires 17um
The top board is lined up with the top of the chip

- Thinner wires,
- If we can remove the HV pad from the first chip and spread out the SPI pads, that will provide more space for wirebonding

Need mechanical drawings - for v3 as well as for v5, for placement
Need envelope drawing for clearance

SPI pads with a wirebond footprint are 40um, it is hard to wirebond 6 wires

Tony - Forest was thinking about using the shaping parameter.. Not ideal, but with v3, we don't have much of an option

Will have to see if we need to add anything for the flex part - makes the tool bigger

Can use a clip or something instead of a vacuum

Tony

Past experience - Vias are failing one way or the other
Vias are these plug-filled or edge-plated vias?
We will use filled vias
One blind via and the other - is this generic
This we what we have one through via and one blind via

Via size, how much is the pad? (more details through email)
6 mil hole and 18 mil pad

10:1 is acceptable for via height vs. width - Steven

Metal listed there - is it from the vendor?
Thickness of metal
For plating, etc.
Foil thickness is dictated by designers
2 ounces (check?) on top and bottom

Limitations of flex PCB

Blind via can increase price (Tim) -
Don't increase cost in this case - they have to do each layer separately in advance - Steven

No vias in flex region

Polar drawing for actual vias (to be provided)

3D view of wirebonds (to be provided)
Need wirebond mapping and also pad details

Tony
Vias at the edge of the metal layer
It should be fine

Separating little triangles
Not aligned

High-speed signal and LV are not aligned
High-speed signals are very well isolated
Routings
Low inductance path

Islands of power - what is edge gap?
3.8 mil ~ 100 microns

High-speed track a gap to control the impedance
The width of the traces is different

Different thickness is needed in the rigid vs the flex region

Gerber files -

Soldermask in SPI traces - prevent shorts and corrosion
Concern with creating another impedance with the solder mask

Vias filled with silver epoxy

Signal loss measurement - during QC - try to do that - need test fixtures

Need to cross-check numbers on slide 18. Seems very low. - Steven

Tony - questions (email)
We do have a standard for creating coupons for everything
Pilled coupons, vias,
Don't investigate every coupon, but check them when we have an issue

dB, what specification do we have
Haven't given any specifications
Which losses are happening from the connector or other material
Intentionally chose low-loss material
More than 20 dB loss, then it won't work

- We should test 12 long boards and try to have a module on each end, and test
- Stayed in a 10% margin, 5% impedance matching

Generic talk on QC in module meeting

1 week to address the questions.
Submit it in 2 weeks from now.

Jul 7, 2025
Attending: Chong, Tony, Aan, Vitaliy,

Argonne -

Tony -
Kirsten received glass dummies
Vitaliy is setting up the DAQ setup
Kirsten is working on the drawings for tooling
Don't know if we have tolerances -
Next week, the collaboration-tracking group will give the requirements from that point
Plate accuracy? If that is limited to some value, then how will that affect?

Written down tolerances!

PNU -

June 25, 2025
Attending: Blake, Maria, Kevin, Manoj, Sanghoon, Tony,

Argonne -
- Gap between chips - tolerance consideration 80 um, not 100 um
- Tooling adjustment - to fit the flex part of AstroLinx during assembly needed a slot to fir the Additional tail
- Review - let us know in advance (July 4th is a holiday, so people can be on vacation) - Tony
- Will share a poll this week to have a review

OSU -
- Blake started an internal review of the board to go over the design again
- Made some changes to the readout board (bridge card). Sent it to Dan to get some feedback about the connection with the AStep FPGA board
- Can we have a presentation to show us the QC procedure on PCB (maybe it is fine to show some other examples) - Manoj

UCSC -
- Kirsten is working on finalizing the design
- Design dimension confusion, but sorted out
- Work on it this week
- Next week will be busy

PNU -
- Scheduled to meet with the company for module assembly - this week
- Share the design and show the glass dummies to discuss

ANL -
- Kevin - The aluminum extrusion will be ready tomorrow
- Done some measurements, check the agenda for the file with numbers

To Do

AstroLinx Review - ASAP
- Quotation
- Order

Coating of PCB? - Sep 2025
- Do we need a coating of AstroLinx due small gap in the overlap?
- Conformal coating

Wirebond Potting?

Module Handling Toolings
- Design finalization - when?
- Quote and order - Lead time?
- Decision pick-n-place vs toolings - Aug 2025?

Wirebond program for v3 modules

June 9, 2025

Attending: Chong, Blake, Kevin, Forest, Kirsten, Maria, Vitaliy, Tony, Sanghoon,

OSU:
- ➔ Blake is in discussion with Greg for fiducials
- ➔ 4 fiducials (will be checking)
- ➔ Forest: xy measurements can vary more or less. Two chips provide two or more points
- ➔ Because all chips have different wirebonds
- ➔ Fiducials are good
- ➔ Vitaliy - if most of them are the same y then we can measure circuit bending
    - ◆ Blake - try to get a comment on whether it is possible to get the same y or x
    - ◆ Finding them on a bonding perspective, it should be fine to have them like it is now
- ➔
- ➔ PCB overhang on the edge of the chips
- ➔ The slide show is just a representation and doesn't represent the actual placement
    - ◆ We have to go to the 7/10" (17 micron) wires to get the SPI wirebonding
    - ◆ Shifting to smaller wires -
        - Impedance will be higher for long wires
    - ◆
- ➔ Kirsten - Horizontal position of PCB to be a little bit flexible
    - ◆ The left edge of the chips doesn't need to be tied to the left edge of the flex
    - ◆ How much clearance do we have
        - ●
- ➔ Solder mask opening around pads - 1 mil wire bond center needs to have 125 um clearance to any solder mask

ANL - Kevin
- ➔ 6 weeks ago - prototype test articles
- ➔ 3-piece test articles
- ➔ Received last week
- ➔ We pull out each of the 3 pieces - all slide together - very good
- ➔ Relatively small
- ➔ Want to do some measurements
- ➔ Unfortunately, these are the ones that we might not use
- ➔ Next iteration - should be used
- ➔ ~2m long
- ➔ ~needs to be cut into the module sizes
- ➔ Tony - don't know the best method for extrusions - how much precision we get
    - ◆ Al piece has to be longer than the chip's length

- Accuracy at end chips needs to be < 30 microns

➔ Misumi Pins - place chips repetitively with an accuracy of submicrons
- Haven't shown any wear but if you do it right you can change them
- Different types graphene ones - screwing ones
- But haven't seen any issue with ATLAS 100-200 times
- The question is how many copies of these plates we need
- Haven't placed the order with this precision in a while
- Need to create prototypes to get them (Berkeley was doing it)

UCSC
➔ Vitaliy - Kirsten shipped out glass chips
- Sanghoon got a message from FedEx - it was delivered to PNU, but somewhere else building or office

PNU
➔ Sanghoon
- Module and Stave - when the glass dummy is received, will contact the local company, worked together for ALICE, and talk to them

➔ Ask to get some design files for the modules to discuss the pick and place machine

General
➔ Tony - Need to-do list
➔ The coordinate systems
➔ Depending on that, get tolerances, quotes, etc
➔ Order - v3 and v5
➔ Aug - design ready - signoff
➔ PED or PREP

June 2, 2025
Attending: Manoj, Chong, Tony, Blake, Kirsten, Forest, Sanghoon, Kevin,

UCSC:

We need fiducials for feature findings
Added to the hybrid in the top layer - gold metal dot 200 um
Plus sign - sometimes it doesn't like - bonder program alignment

Vias - drills are not aligned correctly sometimes, so they are not good
Blake will also prefer a circle
Are there any reasons we shouldn't ground the fiducial
If they stay in the right dimensions, no issue with grounding them
The bigger the spacing between eye pads is better

The last chip hybrid is shorter to avoid collision with the flex part of the adjusant module

Need tolerances on the module base plate

Module extrusions are at Argonne but have not been received yet. Kevin will be checking them tomorrow

This will allow us to inspect tolerances

OSU -
Blake thinks Chip starts after the AstroLinx edge
Greg will send out the files

For review -
Evan vandaval
5:45 later time - if Greg will be presenting

We just need feedback from the design in the Box and to schedule the review
Would like Kirsten to sign off
Initial review of readout board - bridge card (given feedback to designer) - approaching submission (put it in the box for review)

May 12, 2025
Attending: Manoj, Greg, Kevin, Tony, Sanghoon, Chong, Bobae, Maria, Forest, Kirsten

Agenda:
Preliminary design of AstroLinx
Status updates

OSU
AstroLinx design is ready for review
Go over the slides and provide your inputs

UCSC
Kirsten received the glass dummies
Need shipping address
Look into the details of what we want, and look at the pickup point

AutoCAD
What format? Kirsten will be emailing it - done

PNU
Waiting for v5 design changes to fit 2cm x 2cm - ask Nicolas

Apr 28, 2025
Attending: Manoj, Chong Kim, Kevin, Tony, maria, Bobae

Agenda:
Preliminary design of AstroLinx
Status updates

PNU -
Dummy chips module production - Possible to fabricate (for all sites) in South Korea.
- Last week, the national conference in South Korea
- I found the design file in the box. Today, I'm sending the design file to the manufacturers.
- Dummy - go with final chip dimensions and give a pad of v5 (for mock-up)

UCSC -
- Glass chips for dicing (1 week for delivery)
- Need addresses to send
- For Stencil, the company needs a diagram for 100 μm bars
- Need bonding diameter
- Make some version of handling tools
- Learn more with the right chip gaps
    - But going with a larger gap gives a more comfortable start
    - Should have a meeting to get the references correct for module assembly.
- Sanghoon - also trying to test another glue (but just make sure radiation hardness is suitable for chips, for AstroPix as well as ALICE) - ITS3 uses ARALDITE-2011
    - Do some tests this year
- UCSC did some glue tests (list of everything available can be shared) (40 min)

After meeting email from Vitaliy (Thanks, Vitaliy)-

Tony mentioned an interest in rad-hard glues. To that effect, I uploaded a couple of presentations to the Box location "BIC Modules and Staves / Assembly / Glues":
- One is from our studies for ITk Strips. (Note that Epolite and Polaris glues were discontinued since the qualification.)
- Another overview is a CERN seminar from people qualifying for glues for pixel assembly. They generally refer to high-radiation environment, but there is also a reference to older CERN investigation for lower dose.

Is the interest in rad-hard glues due to overlapping work with other project(s)? What I recall for BIC is 1 krad per year (or lifetime), which is rather "small". If this estimate is updated, that would be useful to know.

Apr 14, 2025
Attending: Manoj, Blake, Kevin, Sanghoon, Vitaliy, Bobae

Agenda:
PED/PREP schedule discussion for the modules team

PED -
With the issues from workshop, it is not possible to have a review by April 22, 2025
Finish design changes this week
It takes a little longer to finalize the design
We kind of have a preproduction turnout plan, things kind of changed with this board, NASA folk to have everything they want
In the next meeting, we might discuss - making sure we have all the pins we need for v5

Handling tools - start earlier
- Prototyping
- 6 months

Pick and place machine vs. Handling tools -> decision July 2025
Sanghoon -> For ALICE project
- Packaging company - uses pick and place machine for ALICE module assembly
- Dummy module production with pick and place machine for BIC
- Get position precision, time, and production cost
- ALICE module assembly is ongoing for the first half of the year
- Sanghoon will get back with more information to help with decision
- Potential issue
    - The cure time of glue requires holding the chip in place for the cure time
    - This makes it difficult for auto-assembly
    - It depends on what kind of glue is used, what the cure time is?, whether it fit well with thermal conductivity, radiation hardness
    - The company is building some tooling so that the chip is held in place during cure time using some vacuum tools
    - Sanghoon will find the information and get back

Pre/post protection - wire-bond potting, PCB coating (Parylene vs. conformal coating)
- For wire-bond potting - have experience with Sylgard (Dow Corning Sylgard 184 /186 Silicone?).

Module Assembly (workforce for UCSC)
- For preproduction, the quantity of modules is significant to conflict with ATLAS production at UCSC.
- Don’t have the human power to deal with high-quantity module assembly
- After ATLAS production, it will be much better (**3 years from now, i.e. 2028**)

- Planning for half sector (Manoj)

- 6 layers i.e. 50 staves
- But we need only four layers, i.e. 28 staves
- ~350 modules with 3 sites

Mar 31, 2025
Attending: Manoj, Tony, Blake, Kevin, Vitaliy, Forest, Kirsten

Agenda:

Questions from Forest (will redirect to Steven and Blake)
What is the reasoning behind choosing this connector?
Do we have any experience using this connector?
How many times the connectors can be used?

OSU

Presentation during In-Person meeting
Design is ready - review internally
Work on updates after that
Discussion about possible signals needed
Branches for each of the module
Got the stack up from a vendor
Rigid-flex - trying to use materials with minimum loss

Tony
Assuming for connector losses?
Not considered any loss for connector
In the past seen connectors with loss - 3 dB/connector

Kirsten
- Need pickup area - 4-5 mm2 at several places.

Tony
Copper balancing for glue balance.
The bottom layer is mainly copper-filled - Most likely ground (some routing there, chip select, and power)

Transmission frequency - 20MHz (highest blake could find, everything was 20Mhz, something with 3.125 ns)

Howard Johnson reference - 2 m with 20 MHz will be dominated by LC transmission (Vitaly)
- Rise time and fall time will be affected
- How fast can you get an eye diagram

Fabrication needs to be decided -it depends on the funds.

The flex region needs some space for bending radius - the jumper is another option, but it will double up the losses connector.

UCSC

Kirsten - find the glass vendor.
Brainstorming - relevant aspect of handling and wirbondings

Mar 17, 2025
Attending: Manoj, Bobae, Kevin, Tony, Forest,

Agenda,
Module Design
Module Stave design ideas
Astrolinx
Dimensions and location of PCB
Assembly for ALICE?

Wire bonds are good with 45 deg angle
Small mockup of pad geometry - to see if wire bond is possible
Data connectors provide datasheet
Forest sent 45 deg clearance requirements for wire bonding (from lower to higher height)

V3 and v5 chips are different sizes from the final chip; v6
Ask for wirebond plan to OSU

Carriers

UCSC -
Waiting on drawings
Tooling will include -
Module assembly
Bonder (similar)
Pickup
Do we need tools to move the module?

Designing holders - write down what we want to do. It is more complicated than something attached to the module (it comes off and on). Think about the purpose of each tool and figure out extra features

Think about permanent deformation from the tools.

Write down purposes for tools.. numbers, names…

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Mar 3, 2025

Updates at Argonne

- Module design
- Wirebond discussion
- SPI pad wire bonds

Wire-bond plan - request to OSU
HV bonds - not bad (300-400V)
Wirebond crossing

SPI staircase needs the other way round - talk to Nicolas
HV away from SPI
Chip-to-chip case minimum case
~1 mm

OSU
Pads for the first chip are routed
Greg last week updated the design
Flex region four-layer board
Rigid region eight-layer board
Power regulators for all four voltages for v3
Select solder bridges -
Connector on the bottom - upstream connector
The connector on the PCB is a downstream connector
Used voltage regulators from 9chip pcb
Voltage drop along the stave
516 mV drop across the stave
6V is good but can we do 9V?

- 5V doesn't seems feasible (5V may work - need verification!)
- Power dissipation with 9V is better for stave

Chip select from 12 pin through connector and 1 pin to chip - need soldering
USCS requested wirebond plan with chip overlap
OSU uses Altium
Connector move - inside to align flex part

UCSC
Dummy glass - no response from past company so exploring other options
No grad-student or postdoc to work on DAQ

Feb 17, 2025

UCSC updates -
Ordered some parts of fancy aluminum for toolings.

Need PCB material details for glue studies - module assembly
Blake

- trouble with vendors to get the right stack up
- they gave the recommended stack-up but not good
- signal integrity is not good
- The solder mask is not going to change much

not high requirements - mechanical stability, glue bond,
Blake can provide vender contact
Vitaliy needs to go back to UCSC technicians and check

Glass dummies
500 - suitable option
550 um thickness
/pm 15 um getting quote

1.66mm height wirbondings

- UCSC did some testing like this in the past
- Bond ability to check the length of wire bond
- Test horizontal length and vertical studies at UCSC
- Vitaliy said they can do it

OSU -
Routing the traces and pads
1.2V + 1.8V vssa-vdda can be tied together
18V supply
Which pads are needed or not needed - provide the list of pads to Blake (For Manoj)
1.6 mm in height, the pads are vertical - wire bond strength will be weak. The angle is mechanically weak
The angle of approach should not be 90 deg but less for wire bonding
For vminuspix voltage of 0.7 V - a voltage divider can be used

Comment on Schedule -
Bootstrapping timeline

Feb 3, 2025

Timeline and structure
PED
BIC workshop - most likely early Apr

Updates at Argonne -

- Progress from Nov - Dummy Module and PCB test module 🎉
- Kevin sent the first CAD iterations with a step file from Blake
- Next steps
    - Dummy mockup
    - Testing of PCB board
- Blake
    - checked file from Kevin
    - Rework and send it back to him

Updates at PNU -

- As BIC astropix side - more testing for wafer testing
- ALICE - Korea involved in module production
    - The module structure is a bit different from the ALICE tracker
    - Working with company
    - Dummy module
    - Position procedures
    - Successfully produced dummy modules
    - The next meeting will shows
- For AstroPix modules - provide design files
    - Can start co-ordinate with company
    - ALICE chip is thicker and smaller
    - The precision requirement for Alice is 10s microns
    - For BIC, it is 50-100 microns

Updates at UCSC

- A bit futuristic -
    - Received prototype boards and chips
    - Can do it by hand
    - Thinking about making jigs, much less handy and more assembly line
    - Borrowing procedure from other projects
    - Glue - Atom Adhesive F112
        - It will be good to share datasheet
    - Glass chips with the right size and thickness
        - UCSC does have vender contacts
        - What to know about glue thickness
    - Solder resists going to be on the board
    - The nice thing about Flase glue - Cure time of 3-4 hrs +
        - Can use glue robot, radiation hard
    - What solder resists on the PCB?
        - Blake -
            - Most likely, the solder mask
            - That section of the board will be rigid
            - If you need different material, it can worked out
            - Just need to knowthe material, and we can do studies (Tony)
            - Blake will know it this week (good point to start)

Updates at OSU

- Greg is a lead designer
- Have slides and have a few questions
- Design ideas that will work
- Constraint
    - Stack up that we can use have some flexibility in the region with overlap
- Slides
    - The entire board is 15.52 mm
    - Mockup with material and stack up
        - ~1.6 mm rigid and 300 um flex
    - Designed Half of the board for mock-up
    - 4 data lines, GND is not shown
    - Low and High voltage lines on the left side of slide 7
    - Mock-up with thick PCB of 1.6
    - Budget for PCB fabrication
        - Working on contract for actual board themself
        - If there is material money

PED heads up for next meeting -

- We have timeline
- But we need to know how much we can achieve and how much delay we expect
- Think about when we can finish up the stuff and give a new target according to the new timeline
- More detailed discussion on who is doing what

August 26, 2024

Outline:

Mechanical Design of the Module - Kevin
Flex Design
Discussion of the connector on flex
    Connector width and height
    Wide Flex on module and width can be narrower off the module
    Longer and narrower connector
    How to fit the modules
I/O pin requirements.

Minutes:
Al plate
    - HV bias - Thin layer of Kapton (Vitaliy)
    - Thermal conduction, mounting on tray, alignment, wire bonding support,
    - we haven't finalized the concept for the Tray (Sylvester)
    - Steven - get rid of the Al block and mount the chip directly on the Tray

- Let the PCB be your rigid support - Steven (anyway there is a vertical size constraint).
- Optimization - assembly - Steven
    - That means we are assembling a full tray
    - Stability of full Tray (Vitaliy, Tony)
    - Vitaliy - 1 mil thick insulating layer is sufficient
    - Module PCB
    - Mount 9 chip on the module - test it
    - build N modules and test them at a time and then assemble - Vitaliy

Flex Connector

- Why the range of pins 57- 87 (Steven)
- Need more gnd pins in between
- Impedance mismatch (Blake)

Steven Slides

Communication protocols -

I2C -
Common interface for microcontrollers
2-wire interface -> bi-direction data and clock
Speed 100kbps to 3.4 Mbps over 4 meters (increase it if uses directions differential repeaters)
Single line - no impedance control, not much termination, single ended
Only talks to one device at a time (like SPI)
But can have 128 devices on the same bus
Block diagram for I2C bus (slide 3)

- controller, devices, branching structure (pullup resistors)
- It cannot be implemented on PCB precisely as shown in the block diagram; it is more complicated to make tracks on PCB as it introduces issues
- Special techniques to use the multidrop data lines
- Controller send the messages

SPI

- 3 or 4 wires
- higher speed 1 - 20 Mbps
- 10 meters and if convert it to differential bus it can go upto 100 meters
- one device on the bus at a time - separate clock line,
- shared bus
- - need active low signal for every device - chip select
-
- This is a MultiNode parallel method
    - Simulation required - multi-drop distribution
    -
- Daisy chain (not necessarily exactly the same as for AstroPix, but the basic logic is somewhat similar)

Single ended to differential needs differetial driver chips (slide 8)

Chip select - Dc line - very slow
Chip select - how does it work? Can it be serialized?

- If we do not have enough chip select lines, this system might not work
- Multiple modules (12) come to the end of the Tray card
    - If we use single-ended transmission line the design structure is achievable (slide 11)
    - Should do that
    - At least 16 lines to have one stave single-ended
    - Install some multiplexers
        - And use I2C
- Multiplexer for chip selected needs to be single-ended
- We can look at multiplexer speed - hits in multiple modules
- Are we using interrupt?
- Decisions we make now will have an impact later
- Conservative now for the module design on flex PCB - and in future make some compromise…
- Vitaliy
    - Differential - way too many lines
    - Single-ended - we might have cross-talk
        - Can mitigate cross talk with good pcb design (put grounds)
        - Can put GND between pins (also true for differential) - Steven
    - Feasibility (way to many lines)
        - Width of the pins on connectors
    - Difficult to assess theoretically
        - Rule of thumb - differential work better
        - Differential for clock and data and single-ended for chip select
    - Cross talk and noise induced by the lines (how much space between lines and chips)
    - Not constraint on space, drive with constraint on interfaces (connectors)
    - Smatech has ground blades instead of gnd pins
    - Considering 20 lines are still a lot
    - On the order of 30 pins, can consider
    - I did not even think about custom connectors
        - 3-4 years of development
        - Commercial solutions
        - Which one might work for these operations
        - substantially smaller than LPAM connectors
    - The impedance of the connector must be very low if it is mounted on silicon - mate/demate them.
    - Hard to solder, hard to mate - demate
    - Need serious structure underneath the connector to support demating
        - Better smaller options are available
        - Change the design of vias, change glue, etc.
    - The mating force on the flex is different depending on the gender of the connector.
    - From experience, the male connector has a lot of force.

Reach out to KIT with questions related to the Chip interface.

Steven will look into more connector options (significantly smaller)
Revisit the Pinouts for the End-Of-Tray card - - Module interface.
Kapton (insulating layer) in between AstroPix Back (HV) and Al-plate
Steven - get rid of module Al base plate on mount chips directly on Tray
To have a module reworkable, test a system at Module level
Optimization - test stability may not be ideal, if some modules are bad they can be replaced easily

Questions:

1. Chip select single line is connected in series for different chips in daisy chain. Each chip needs to get the active low to send the data - how does this system work? Can it be serialized within the module (Manoj - It goes low for all chips in the daisy chain)? How do we know which chip needs to go active low when data arrives?
2. Chip select needs to be single ended instead of differential - which will be slower but should work
3. Do we need Interrupt lines? Without interrupt you can hold these things even 20 Mbytes. If we have interrupt line then we are back to 30 pins datalines
4. Differential for clk and data, single ended single for Chip select?

Answers:

1. Chip-select: It is daisy-chained on the modules (for 9 chips). The chip-select signal is propagated/buffered from chip to chip. So if we set the chip select as active-low, other chips in the chain are also set to active-low. So, we can put the entire module as active-low and not an individual chip. The broadcast commands can be sent to the individual chips using their ChipID. The chip responds, and records hit independently of chip-select status, and the chip-select active-low is only needed for the SPI communication.
2. Interrupt: The data can be read out without connecting the interrupt lines. The interrupt line is a status output signal showing which module you want to read out and for how long. Of course, one can apply a round-robin-based readout scheme and read out until you get something like 9*2 IDLE Bytes and then hop to the next module. The chip can generally store one hit for every pixel because each pixel has one hit buffer. Additionally, there is a small readout fifo that can store 8 hits. If this fifo is full, the hitbuffer readout stops. Now, if a pixel gets a hit B and the hitbuffer already stores a hit A, then hit B will be lost.
3. SPI bus: The status of the SPI FIFOs for incoming and outgoing data in the chain, as well as the readout fifo, is considered in the interrupt logic. Interrupt still has to connect for all chips even if we only want to look at the SPI chain FIFOs because one chip does not know if the other chips have something in their SPI FIFOs.
4. Differential vs. single-ended: AstroPix currently only uses the single-ended or differential interface. Nevertheless, as a workaround, we can use the differential interface for 4 SPI lines (1 CLK, 1 MOSI, 2 MISO) and connect SPI_CSN_N to VDD/2 and drive SPI_CSN_P as a single-ended 1.8V CMOS Signal. On the other hand, there will be a pad "use_spi_diff," which allows either the single-ended interface or the differential interface for all 5 SPI buses.

2 MISO needs to be differential

It needs to be tested.

Other SPI line's differential N pin needs to be connected to half the supply voltage (VDD/2)