

## **April 13, 2026 - Assembly Tooling Review and general meeting**

Attending: Kirsten, Tony, Jessica, Forest, Kevin, Tim, Manoj, Sanghoon, Chong,

The gap between chips, 100 micron is too hard

- Increasing the gap will make things easier

Kevin

- machine shop - company makes tooling for silicon carbide
- Made prototyping
- Tolerances are too tight - can they make it?

PNU

- Adaptor card - working on circuitry - finishing this week. Will check with him
- Fabrication is faster - it is already prepared in the company process - 1 week or 2
- Software - progress about software test routine
  - Chip can communicate with the software
    - Take the file, injection, and threshold
    - Need to add more routine
    - AStep FW/SW

## **April 06, 2026**

Attending: Manoj, Tony

USCS -

For a chip pick-up tool

Working on another option instead of screws/pins to hold them together

Maybe magnetic posts

Printing a few test articles with the new design

Review next week, okay

ANL

Kevin moved forward with Al base plate order

Lead time delivery June 2026

## **March 30, 2026**

Attending: Manoj, Chong, Tony, Kevin, Sanghoon

PNU

- Adaptor card is being developed.
- Meeting tomorrow with the engineer
- Will test in the lab without a full setup
- Testing using the AStep - DAQ chain is working
  - Script and injection working is tested

- If this test can be tested using a bare chip

#### UCSC

- 3D printed parts
- Aluminum extrusion doesn't fit
- Review in 2 weeks
- Encapsulation
  - Start discussion
  - Write down the requirements
  - In the assembly procedure
  - Dedicated discussion

#### **March 23, 2026**

Attending: Manoj, Chong, Sanghoon, Kevin

#### PNU

- Probe card adaptor - the engineer started work
  - discussed a few things
  - Found a bug with the current version
  - Power issues - can not be tested
  - Test signal pins one by one
- Trouble with AStep SW/FW
  - AStep software is not very well prepared at the moment
  - Can't use it directly for this task
  - Can make some progress this week
  - If it still gives issues, then roll back to Python-based scripts

#### ANL

- Meet with Kevin and Tim to go over the design files of tooling and basically what we want to achieve with these toolings

#### **March 16, 2026**

Attending: Manoj, Tony, Kirsten, Sanghoon, Adam, Bobae

#### UCSC -

3D printed everything

Will 3D print a hybrid with PLA to play with it

Still need a solution for the chip location

Next week at CERN for ITkWeek

Extrusion to UCSC and dummy modules.

#### PNU -

Working on the AStep testing setup

The probe card touch-down adaptor is going back and forth.

#### ANL -

No updates

### **March 9, 2026 (Cancelled)**

Attending: Manoj

Cancelling the meeting

### **March 2, 2026**

Attending: Tony, Manoj, Bobae, Sanghoon

ANL

- Testing the external clock with the latest bit files
- Preparing for the March Hall D beam test

UCSC

- 3D printed toolings are delivered
- Hybrid pick-up
- Chip pickup
- What do we need to go into the review for toolings
- Organise a meeting on glue (robot, working glue life) and encapsulation (is it possible?)? - understand what constraints are

PNU

- No particular news
- Chong continued testing the chip for Chip QC - successfully tested using AStep FW/SW
- Sent 9-chip PCB boards

### **Feb 23, 2026**

Attending: Chong, Bobae, Manoj, Kevin, Tony, Kirsten

UCSC

- Wirebond test on Extrusion
- Glass and dummy chips - works well
- Pull tests were good (~9-10 gms)
- PCB to chip wire bonding
  
- Encapsulation - not obvious
- Decision on the glue
  
- Toolings

- **Dedicated review for Toolings**
- 3D printed tools for Review
- 3 copies single set by in-person meeting (June 16-18)

#### PNU

- Contacting probe card engineer - no promises, but will work on it

#### ANL

- Testing module PCB, preparing for test beam
- Received AStep FPGA boards - 5 (two will go to PNU, 3 are available)
- AStroPix v5 fabrication began at AMS (making masks), another foundry option, LFoundry - 2 x 3 cm<sup>2</sup> reticle size possible

### Feb 16, 2026

Attending: Chong, Manoj, Kevin

#### PNU

- Holiday
- Plan to continue testing
- Probe adaptor card - engineer - still haven't started working on it
- How the V5 architect is designed (hit buffer for each pixel)
  - How signal sent to the digital periphery
  - Any chances of a pile-up for multi-pixel injections
- AStep firmware - discussion

### Feb 11, 2026

#### DAQ-Module joint meeting

Attending: Chong, Halen Davies, Akshaya, Beattite, Regina, Adam, Blake, Manoj, Adrien, Aram, Dan, Shefali, Shinhyungkim, Zisis, Maria,

Introduction to modules - Manoj

9 AstroPix chips on module

12 modules on Stave

6 - 7 Stave on a tray

2 trays per sector layer

Introduction to AstroLinx - Blake

question - Driven, source series termination (Adam) For signal runs through cables that are not daisy-chained

Signal loss at the end of the chain

There are some termination resistors

ComPair2 FEE -

Shown at AstroPix workshop

Lattice CErtusPro  
DC-DC converters for housekeeping  
20-pin connector with 20 lanes  
DC to DC screenshot  
Lanes with a bus

ComPair2 is switching to the Lattice non-pro version, so downgrading to use free licensing for flashing the FPGA

How we would like to approach EPIC design is to take this design or take a smaller version of the FPGA

Match the new form factor.

12 cm to 16 cm trapezoid for the ETC card

Adam -

Can do a lot of options on PPT  
But need dxf from the mechanical engineer

Time slot

End-of-sector box meeting at 8 am  
But we can set up a doodle poll for the new slot.  
Figure out the slot.

## **Feb 9, 2026**

Attending: Manoj, Chong, Bobae, Sanghoon, Tony, Kirsten,

PNU

Probe card chip testing procedure

Tentative plan in four parts

Initialize - FW/SW configuration, touch down, power up

Test -

Analysis

Cleanup

ALICE ALPIDE - also upload the results to the database - provide a summary report

Initial test items and injection studies

## Initial test items

- **Initial test items plan to implement**
  - **Communication check and Register R/W**
    - a. [Board ↔ chip communication](#) (to check if the chip is alive)
    - b. [Register map check](#): key register values write/readback
    - c. Record: bias voltage, current, temperature, fw, entire register map
  - **Basic performance: require parameters study and tune**
    - a. [Noise scan](#): # of hot/dead pixels, generate occupancy map
    - b. [Injection scan](#): by using low and stable event rate
    - c. [Threshold scan](#): generate s-curves for multiple points
    - d. Record: results plots generated by ROOT
  - **Stability**
    - a. [Generate 2D hit map](#) in “standard” setup (e.g., bias -200V, threshold 200 mV, runtime 30s, etc)
    - b. Repeat at least 3 times and check consistency
    - c. Record: hit maps

## Injection studies

### Single pixel

### Single row or col

### All rows and cols

4 / 5

### Injection study (2/3)

- **Rate capability of single pixel (c10, r10)**
  - **Official info vs. Measurement**
    - a. Spec: 4 Hz/pixel (arXiv:2511.05639)
      - This limit seems like operational condition, rather than the physical/technical one
    - b. Parameters relevant to event rate being injected (astropix-python):
      - i-1.  $inj\_period$  (0, 255)
      - i-2.  $clkdiv$  (1, 65535); default 300
      - i-3. Judging from data,  $f_{inj} = \frac{f_{clock}}{336 \cdot clkdiv \cdot (inj\_period + 1)}$ ,  $f_{clock} = 100$  MHz, given by Nexys-video
    - c. Conditions: single pixel injection (c10, r10), -150V (bias), 400 mV (threshold), 500 mV ( $inj\_voltage$ ), 10 s (runtime)
    - d. Repeated same measurements for 3 different chips (w102s08, s10, s12): consistent

inj_period	clkdiv	n_lines	n_readout	File size (kB) (* csv decoded)	Contamination	Rate (Hz)
0		65,144	1,666	3,742	?	?
10		2,495	1,247	141	N	~125
100	300	259	239	15	N	~13
162		159	79	9	N	8.0
255		101	50	6	N	5.1

### Injection study (3/3)

- **Rate capability of all pixels**
  - **Scanned inj\_period and clkdiv**
    - a. Data starting to be contaminated (truncated packet, corrupted row/col consistency, readout overlap, etc.), if the  $inj\_period$  is lower than 162 (event rate is higher than 8.0 Hz)
    - b. For chip performance test purpose,
      - i-1. 7 ~ 7.5 Hz injection rate
      - i-2. A few tenth seconds of runtime
    - c. If necessary,  $clkdiv$  can be utilized for extremely high/slow event rate
    - d. Tentative test procedure: default (7 Hz + 30s) + precision (only when the status looks suspicious)

inj_period	clkdiv	n_lines	n_readout	File size (kB) (* csv decoded)	Contamination	Rate (Hz)
100		9,096	259	498	Y (substantial)	~13
129		7,065	201	386	Y (substantial)	~10
162	300	5,682	161	310	Y (slightly)	8.0
		3,885	114	210	N	5.1
255	600	1,821	52	98	? (not checked)	2.6
	150	7,141	205	389	? (not checked)	10.1

LAST SLIDE

## ANL

9 chip updates

First module #4 works with chip 8 gives 0 ToT

Two more modules, 7 and 8 working after the correction to PCB - chip 2, 5, and 8

don't work

Plan for testbeam

10MHz with private code

40MHz needs to be checked

Need longer cables between SFILs

Feb 2, 2026

Attending: Manoj, Chong, Bobae, Kevin, Blake, Jinhyun

## PNU

- Jinhyun joined the PNU team (graduate student)
- Probe card to perform chip test
  - No progress
  - Contact the electronics company to get the status
  - Waiting for a reply
  - Preparing the electrical contact routine - end of this month, Feb (but busy person)
  - Regina and other members want to touch base with the Astep firmware to use a common decoder
  - Performed actual routine to perform the injection with astropix-python - inj for the whole row/col - this week's plan
- Sanghoon
  - Will send AStep FPGA boards next week
  - Will fabricate a base plate with a sharp corner to test assembly precision
  - Let Manoj know if round corner base plates are needed to do additional tests
  - Meeting with the company next week

## Oklahoma

- SoW - finance person helping with BNL to get it out sooner
- Placed all the orders
  - But they don't want to pay the PO until they get approval
  - Start getting boards in a couple of weeks

## ANL

- Testing the quadchip and 9-chip PCB board
- Beam test at Hall D in March (10th?)
- A Step board and a quad chip
- Comparison with the previous KEK beam test
- Have a readout rate limit and a count rate limitation
- Long-term FY26
  - AstroPix with ETC
- One 9-chip module is working
  - One more under debugging
  - Tried to test module 7 and saw some solder detached, and need to check
- Send Schematic file link to Blake to look into HV biasing issue

## Jan 5, 2026

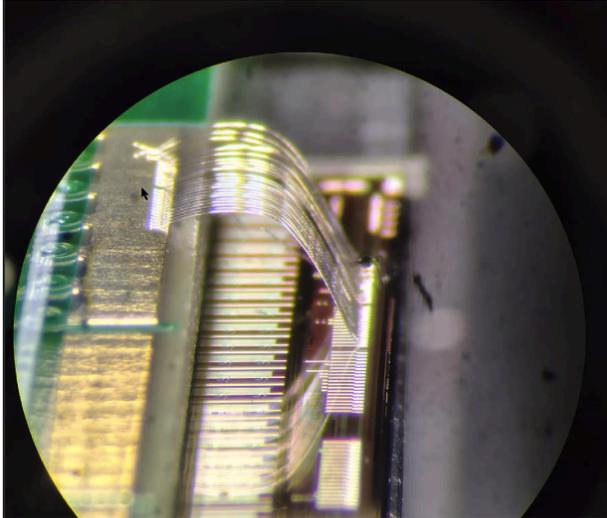
Attending: Manoj, Chong, Bobae, Kevin, Jessica, Sanghoon, Tony,

## PNU

- Adaptor card starts end of January and is delivered at the end of February
  - Fabrication is very straightforward
- Sanghoon needs a "working file" for the automated population of PCB
- Dummy chips this week (300)

## UCSC

- Kirsten was working on drawing - 3D printing - half of them done - adjusting the other two
- Bonding trials - good bonding
  - 9 gm



Wirebond from bottom to top or otherwise -> top to bottom (more common practice)

Stencil to adjust spaces between chips

Movement of chips - holding the chip down

Fix the glue

Try a couple of things and see what happens

ANL -

Bobae

- AstroPix chip testing
- 3 quadchip working well
- V4 chip not responding to injections
- Hgc3roc for synchronisation
- Two more 9-chip boards need to be debugged

**Jan 5, 2026**

Attending: Manoj, Bobae, Chong, Tony, Sanghoon, Kirsten,

Workfest -

workfest for wafers and modules for BIC imaging layers.

Discussion about AstroLinx and ETC with people from NASA and Oklahoma State.

Wednesday afternoon?

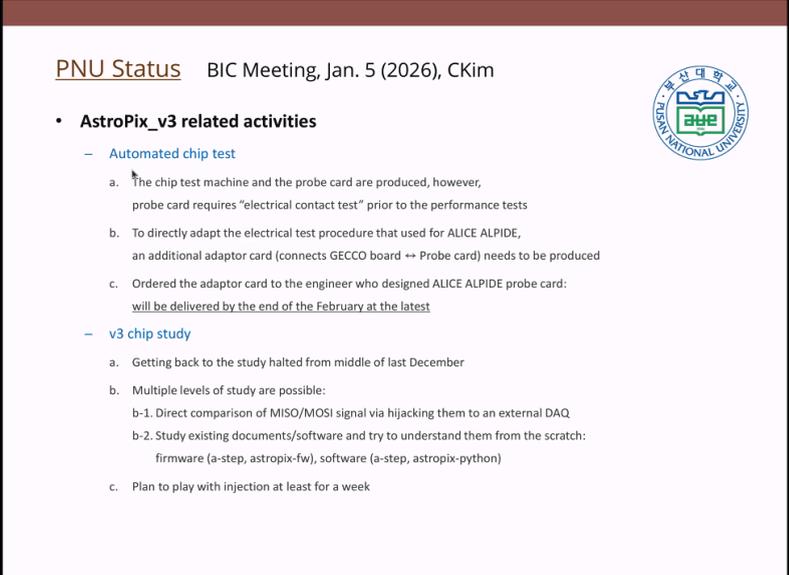
Tooling and wire bond challenges with module-based design

Mitigation to achieve a 100-micron gap between chips

Keeping the option to have a pick-n-place machine for assembly as a backup plan

There is someone from UCSC coming, and we will be discussing tooling with them. If either or both of you can come, we can plan something to discuss the interface between AstroLinx and ETC with NASA people, and I can see if they can come.

PNU -



PNU Status BIC Meeting, Jan. 5 (2026), CKim



- **AstroPix\_v3 related activities**
  - Automated chip test
    - a. The chip test machine and the probe card are produced, however, probe card requires "electrical contact test" prior to the performance tests
    - b. To directly adapt the electrical test procedure that used for ALICE ALPIDE, an additional adaptor card (connects GECCO board ↔ Probe card) needs to be produced
    - c. Ordered the adaptor card to the engineer who designed ALICE ALPIDE probe card: will be delivered by the end of the February at the latest
  - v3 chip study
    - a. Getting back to the study halted from middle of last December
    - b. Multiple levels of study are possible:
      - b-1. Direct comparison of MISO/MOSI signal via hijacking them to an external DAQ
      - b-2. Study existing documents/software and try to understand them from the scratch: firmware (a-step, astropix-fw), software (a-step, astropix-python)
    - c. Plan to play with injection at least for a week

End of February - the adaptor card will be delivered to PNU

Data waveform structure for chip testing firmware

Sanghoon -

A Step hardware PCB

- started to get quotes
- Buy the components (difficult to make big contracts)
- Start with 5 before Feb
- The new fiscal year starts in March - then do the remaining

Dummy chips

Start sending them

Bobae -

UCSC -

Send Kirsten updated drawings

3D hybrid tools

3D print samples of them -

<https://anl.box.com/s/g9zgrrjtgg3ll050u2tk8yabt4w4yquo>

All the drawings are consistent with the center of the AI plate

**Dec 15, 2025**

Attending: Manoj, Kevin, Tony, Chong,

Workfest during ePIC meeting -

Email with details to Tony+

Kevin -

Drawings with the latest AstroLinx board and fitting in the envelope

Include glue layers

Latest AstroLinx PCB

Centered on Module

0.2 mm lost in reverse flipping

Connector flex PCB is 13mm -> can be smaller

Vendor for extrusions - nice job - in specs and tolerance

Current Tray with one wide piece

The lightest piece can be smaller than 4 inches

Two-piece Trays

One more thing to do before attaching them

Bond them permanently and handle them as a single piece

UCSC -

PNU - Chong

- Probe card - contacted design engineer
- The engineer confirmed that he will start working on the design
- Adaptor card touch-down method
  - Electrical contact procedure to start testing
  - Fastest expected time middle of January next year
- Resumed testing on the v3 chip
  - A few questions - raised during the AstroPix meeting
  - Resume the study after Christmas
- Probe is under testing
  - Assembly completed - 3
  - Sent to the chip testing company
    - Connect it to the machine and test it
    - The chip testing company is waiting for the electrical contact procedure

**Dec 8, 2025**

Attending: Manoj, Chong,

**Nov 24, 2025**

Attending: Manoj, Chong, Bobae,

3 probe cards fabricated - expected early next week (end of this month)

Write to Nicolas and Richard to have a meeting for the Probe card discussion

**Not gonna take**

**Nov 10, 2025**

Attending: Manoj, Chong, Bobae, Blake, Tony, Maria

**OkState -**

Quantity 30 - 10k

With the other 2 items - 16k total

Is it for everything, fabrication, and population? - It is the fabrication and assembly of a rigid board - 10k

40-pin to 60-pin

AstroLinx PCB is designed

Procurement process started for AstroLinx Rigid board

Final changes for flex and readout board

Set up the review when that is done

Order placed before the contract ends for current funding

Some QA/QC test stand options are a little bit different from what we are used to

Because of the wirebond pads

What is the stack?

1.2 mm pcb + 2 mm connector + 0.3 mm (0.5 mm stiffner)

Greg sent out CADs to Kevin and Ron to check if they fit the envelope (maybe he didn't).

**PNU -**

Probe Card - is with the needle assembly company - by the end of this month

Preparing software - Python software is going slowly

DAQ and decoder with C++

Received the AStep FPGA PCB and will take a look at it this week.

Email about dummy chip - produced

10 6" 6-inch wafers are produced and diced.

Dummy module assembly - AI with the company, and check the quality and procedure.

Please send us 6 wafers with dummy chips.

## **Argonne -**

Had a meeting with the Representatives from the Aluminum extrusion company.

Kevin, Tom, and Ron joined

I was there for a brief discussion in the initial 30 minutes

They can not do 0.5mm thin flat edges of the module

They can do a slanted edge and a 1 mm flat edge

They can only do ~4cm wide single-piece extrusion

Proposal-

One-day or half-day workshop - either in-person or remote

Brainstorming all the technical details of the modules and the envelope

Assembly procedures, numbers, etc.

Options for production

## **UCSC -**

We can try to do a tapered edge, and Forest can try to see

Kirsten can design a tapered edge

Try to design with a tapered edge

Final drawing for both - Ron and Kevin send the final drawings of both designs of Staves

Did not get a chance to do the cantilever test - wirebond

**Nov 10, 2025**

## **Modules and Wafers**

Attending: Manoj, Chong, Tony, Bobae,

Agenda for this week -

News from the project side, summary of the joint meeting between Modules and Mechanics

Update on AstroLinx PCB, Readout board, and Flex Jumper

Update on assembly toolings (note - we are waiting on the extrusion profile from mechanics)

AstroPix chip testing stand and probe card

Chong - Sanghoon is in Conference - organizer for conference in S.Korea - so may not join

Wafer -

PNU -

Chong - Still ongoing, probe card and chip testing system

Probe card PCB is produced

Some of the components arrive internationally, so expect some delay

End of this month to early December

AstroPix Python and FW package

Software - stably run and extract data with existing code

SPI protocol - make sure

No status about - AStep FPGA PCB

Holding at the Customs

UCSC -

Need a conversation about additional space - it is too constrained

Did not follow up on Forest -

Check with in in-hand Al plate and AstroPix

Share AstroPix v3 with 500 um bad chips - will send it to UCSC

Plan a module meeting, brainstorming!

Might invite someone who uses a pick and place machine for strips

One of the Canadian group, or Oxford group, or the Purdue group

Visit the site to learn - before meeting Mathew Jones (Purdue)

ANL -

9chip testing - no slides

Reworking with Sr90 data taking with different time 5sec, 15sec up to 1 hour

Data rate and hits per pixel

1k event per pixel, around 1 hour

Running 3 quad-chip -

Quadchip masking

The new Quadchip didn't work for chips 2 and 3.

Wire-bonding needs to be checked.

**Nov 5, 2025**

**Joint meeting Modules and Mechanics**

Attending: Blake, Tony, Forest, rtkmak, Kevin, Vic, Sylvester, Tom, Manoj, Kirsten,

Old profile has a flat edge -

New profile has wings

- Need flat support and also an edge to align the modules
- The corner at the edge doesn't allow for to placement of the base plate flat
- Another difficulty is that we now have a very small area to put vacuum holes in the middle
  - Chip could rock while assembling
  - Even with tight channels
- Wirebonding
  - Bonding at the edge of the extrusion
    - So not ideal for flat support
- Sylvester
  - This needs to be placed close
  - How hard can the corner be extruded
  - Hard to extrude if it is too thin

Extrusion company in town next Friday - will talk with them and get more information

14th - get profile information

Not meeting before that

Can also reach out to the company and talk to them

Circuit thickness: When to obtain information?

Try to negotiate 0.5 cm space inside of detector - Al plate  
Need to talk to the project.

3.5 mm => 1.2 rigid + 2 mm connector + 0.3 mm

### **Oct 27, 2025**

Attending: Forest, Manoj, Tony, Kirsten, Kevin, Blake,

Agenda -

Tooling updates

Astrolinx progress

9chip PCB testing

PNU

The dummy chip has been prepared,

How many chips are needed for the assembly test?

All wafers are diced, so I can send them after detaching the diced chips from the tapes.

Argonne

OkState

Blake - haven't had a chance to talk to Greg today

The rigid portion is pretty close to done

Flex is being designed

Connector is changed - a lot of the same thing with a longer length, Same height

Stack up a 1.1952 +/- 0.1 mm thick rigid portion

The flex region should be around <0.3 mm

Kirsten -> What is the height of the PCB -> 1.1952 +/- 0.1 mm

Blake -> alignment pins - will check? How much does it stick out from the back of the

flex

No alignment pins on the Rigid part of the AstroLinx

Right now, we have a lot of power planes -> if it is too much copper (testing through pre-production), the option may be to get rid of copper for power is one option in the future

## UCSC

Metaphor: Aluminum for the vacuum - chip pickup tool for now  
Misumi alignment pins - diamond and round edge mixup

Chip pickup tool drawings are pretty much done

The chip alignment tool is challenging

1.3 mm gap for v3 and v5

Stencil tools

Chip Aligner

Option 1

Stencil - challenging for v6, 100 um

Option 2

Vertical slot

Require hand-crafting

Hybrid Pickup tool

2 vacuum pins for the connector side and 3 more along the length

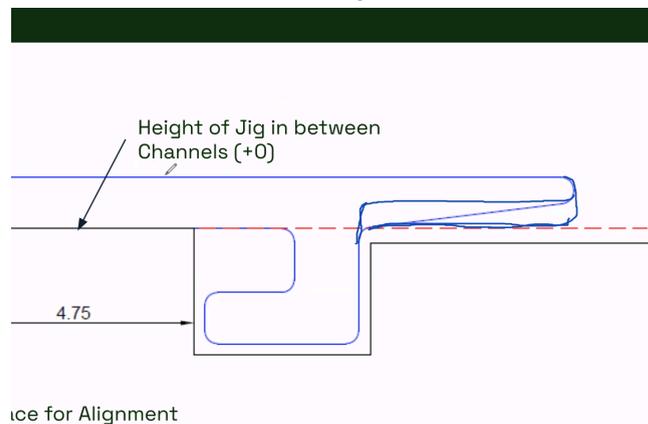
Need connector part number (Blake will provide it)

The extrusion profile was wrong

Concerns with the new design

Edges are at an angle

- So they can tilt while assembly
- Also issue with wirebonding



- 
- Blake - slide 6, tolerance for PCB can cause any tolerance
- Write to Sylvester and Mechanics
- Get input from the Stecil company

## PNU

Dummy chips are ready to be shipped

AstroPix probe card is ready

PCB is ready in two weeks from now

AStep FW/SW run with single chips

I can take the data only once

Have to restart the system

The chip test machine is now being produced and is under calibration and tuning stage - dummy probe card for other chips

Having a meeting weekly

Tony is up

Blake - late time slot is difficult

## **Sep 29, 2025**

Attending: Chong, Blake, Tony, Sanghoon, Manoj, Kevin

OSU

Paused the order

Greg started working on the design - a two-piece module

PCB + jumper cable

Go ahead and switch to the final connector

Put enough pins and route enough traces to connect 12 modules

Chip select and interrupt for 12 modules (vs. 6 modules)

Take out some of the power scheme

Placement of the chips - need a drawing (Kirsten's PPT?)

End-of-Tray Card - haven't started yet, so change of connector will not yet affect ETC design

UCSC

100 micron is difficult

We can't progress the v3 version stuff

Very near future - need to get this done

PNU

Dummy sensors under production

Not able to change the pads

Fabrication of 10 wafers 6 inches are under fabrication

We can use the first production results as a trial for assembly, and after checking the status, we can proceed with the second batch.

ANL

FPGA boards are fabricated, waiting for population

Will send them to PNU

Along with that, we will send one 9-chip PCB - unpopulated

Snaghoon will try assembly and test

If it doesn't work, Argonne will send him a working 9-chip PCB

9chip PCB setup move to cleanroom - Bobae  
Will start testing other boards now.

**Sep 15, 2025**

Attending: Chong, Bobae, Maria, Blake, Tony, Sanghoon, Manoj

**PNU**

Probe card is almost finalized - final confirmation from the company

One try, and if everything works fine

Update later

Started looking around the firmware system

PNU (Yoonha) tested single chip (v3)

No problem so far wrt FW/SW

Plan to write a compatible version with v3 to take data

All chips are v3 at PNU

Can we run FW/SW?

QC test setup - Sanghoon is travelling - sometimes this or next week, ready to test

Probe card ready - need to check leadtime (end of this month)

**OSU**

We are pushing the order through the bridge card

Module PCB - ON hold (what is the new plan?)

Focusing on Review

Blake at CERN next two weeks

**UCSC**

Three stencils

Can't use it for anything

Can do v3 chips

NCE got through today

Kirsten's computer is back with powerful CAD

Working on Hybrid details - placement pickup tools

Longer terms v5 - need to discuss

One stencil with different widths of bars

Very thin stencil, so try out different thicknesses

4 weeks from now, we will go over stencil, pickup tool designs

Oct 13th

**ANL**

9chip PCB testing done with v3

Dry Run - Bobae

Dry Run - Greg

## **Aug 4, 2025**

Attending: Chong, Blake, Bobae, Forest, Manoj, Yoonha, Tony, Kirsten, Kevin

### 1. AstroLinx PCB design signup

Finished the design over the weekend

Few more things to correct - suggestion from Blake

Ground pad extension is still pending

A week and a half to get it on the floor for fabrication

### 2. AstroPix dummy chip fabrication

Chong - dummy chip fabrication - email exchange

They requested the final dimension for submission for 10-20 units

### 3. 9Chip PCB board testing updates

9chip pcb injections

Issues

Lower analog output

No injections at the periphery

Max buffer output

Tony (new design Review comments)

Page 4 Layer 6 copper is missing in some areas (Layer 7 )

Small cleanup

### 4. Assembly tooling updates

Have ordered glass chips with v3 v5

Ordered alignment stencils to place the chips on the extrusions

250  $\mu\text{m}$  to xxx gap

Chip aligned to the bottom left corner of the 20 x 20 pocket

Announcement:

PDR on Sep 17 and 18

Couple talks from Modules and wafers

Modules/Staves

AstroLinx

## 9chip PCB testing (combined with System Testing)

**Jul 21, 2025**

### **AstroLinx Internal Review -**

Attending: Tim, Steven, Tony, Manoj, Regina, Adrien, Kevin, Blake, Jessica, Maria, Dan, Chong, Bobae

Aligned with the left edge

Thinner wires 17um

The top board is lined up with the top of the chip

- Thinner wires,
- If we can remove the HV pad from the first chip and spread out the SPI pads, that will provide more space for wirebonding

Need mechanical drawings - for v3 as well as for v5, for placement

Need envelope drawing for clearance

SPI pads with a wirebond footprint are 40um, it is hard to wirebond 6 wires

Tony - Forest was thinking about using the shaping parameter.. Not ideal, but with v3, we don't have much of an option

Will have to see if we need to add anything for the flex part - makes the tool bigger

Can use a clip or something instead of a vacuum

Tony

Past experience - Vias are failing one way or the other

Vias are these plug-filled or edge-plated vias?

We will use filled vias

One blind via and the other - is this generic

This we what we have one through via and one blind via

Via size, how much is the pad? (more details through email)

6 mil hole and 18 mil pad

10:1 is acceptable for via height vs. width - Steven

Metal listed there - is it from the vendor?

Thickness of metal

For plating, etc.

Foil thickness is dictated by designers

2 ounces (check?) on top and bottom

Limitations of flex PCB

Blind via can increase price (Tim) -

Don't increase cost in this case - they have to do each layer separately in advance -  
Steven

No vias in flex region

Polar drawing for actual vias (to be provided)

3D view of wirebonds (to be provided)

Need wirebond mapping and also pad details

Tony

Vias at the edge of the metal layer

It should be fine

Separating little triangles

Not aligned

High-speed signal and LV are not aligned

High-speed signals are very well isolated

Routings

Low inductance path

Islands of power - what is edge gap?

3.8 mil ~ 100 microns

High-speed track a gap to control the impedance

The width of the traces is different

Different thickness is needed in the rigid vs the flex region

Gerber files -

Soldermask in SPI traces - prevent shorts and corrosion

Concern with creating another impedance with the solder mask

Vias filled with silver epoxy

Signal loss measurement - during QC - try to do that - need test fixtures

Need to cross-check numbers on slide 18. Seems very low. - Steven

Tony - questions (email)

We do have a standard for creating coupons for everything

Pilled coupons, vias,

Don't investigate every coupon, but check them when we have an issue

dB, what specification do we have

Haven't given any specifications

Which losses are happening from the connector or other material

Intentionally chose low-loss material

More than 20 dB loss, then it won't work

- We should test 12 long boards and try to have a module on each end, and test
- Stayed in a 10% margin, 5% impedance matching

Generic talk on QC in module meeting

1 week to address the questions.

Submit it in 2 weeks from now.

### **Jul 7, 2025**

Attending: Chong, Tony, Aan, Vitaliy,

Argonne -

Tony -

Kirsten received glass dummies

Vitaliy is setting up the DAQ setup

Kirsten is working on the drawings for tooling

Don't know if we have tolerances -

Next week, the collaboration-tracking group will give the requirements from that point  
Plate accuracy? If that is limited to some value, then how will that affect?

Written down tolerances!

PNU -

### **June 25, 2025**

Attending: Blake, Maria, Kevin, Manoj, Sanghoon, Tony,

Argonne -

- Gap between chips - tolerance consideration 80 um, not 100 um
- Tooling adjustment - to fit the flex part of AstroLinx during assembly needed a slot to fit the Additional tail
- Review - let us know in advance (July 4th is a holiday, so people can be on vacation)
  - Tony
- Will share a poll this week to have a review

OSU -

- Blake started an internal review of the board to go over the design again
- Made some changes to the readout board (bridge card). Sent it to Dan to get some feedback about the connection with the AStep FPGA board

- Can we have a presentation to show us the QC procedure on PCB (maybe it is fine to show some other examples) - Manoj

#### UCSC -

- Kirsten is working on finalizing the design
- Design dimension confusion, but sorted out
- Work on it this week
- Next week will be busy

#### PNU -

- Scheduled to meet with the company for module assembly - this week
- Share the design and show the glass dummies to discuss

#### ANL -

- Kevin - The aluminum extrusion will be ready tomorrow
- Done some measurements, check the agenda for the file with numbers

#### To Do

##### AstroLinx Review - ASAP

- Quotation
- Order

##### Coating of PCB? - Sep 2025

- Do we need a coating of AstroLinx due small gap in the overlap?
- Conformal coating

##### Wirebond Potting?

##### Module Handling Toolings

- Design finalization - when?
- Quote and order - Lead time?
- Decision pick-n-place vs toolings - Aug 2025?

##### Wirebond program for v3 modules

#### **June 9, 2025**

Attending: Chong, Blake, Kevin, Forest, Kirsten, Maria, Vitaliy, Tony, Sanghoon,

#### OSU:

- Blake is in discussion with Greg for fiducials
- 4 fiducials (will be checking)
- Forest: xy measurements can vary more or less. Two chips provide two or more points
- Because all chips have different wirebonds
- Fiducials are good
- Vitaliy - if most of them are the same y then we can measure circuit bending
  - ◆ Blake - try to get a comment on whether it is possible to get the same y or x
  - ◆ Finding them on a bonding perspective, it should be fine to have them like it is now

- 
- PCB overhang on the edge of the chips
- The slide show is just a representation and doesn't represent the actual placement
  - ◆ We have to go to the 7/10" (17 micron) wires to get the SPI wirebonding
  - ◆ Shifting to smaller wires -
    - Impedance will be higher for long wires
  - ◆
- Kirsten - Horizontal position of PCB to be a little bit flexible
  - ◆ The left edge of the chips doesn't need to be tied to the left edge of the flex
  - ◆ How much clearance do we have
    -
- Solder mask opening around pads - 1 mil wire bond center needs to have 125 um clearance to any solder mask

#### ANL - Kevin

- 6 weeks ago - prototype test articles
- 3-piece test articles
- Received last week
- We pull out each of the 3 pieces - all slide together - very good
- Relatively small
- Want to do some measurements
- Unfortunately, these are the ones that we might not use
- Next iteration - should be used
- ~2m long
- ~needs to be cut into the module sizes
- Tony - don't know the best method for extrusions - how much precision we get
  - ◆ Al piece has to be longer than the chip's length
  - ◆ Accuracy at end chips needs to be < 30 microns
- Misumi Pins - place chips repetitively with an accuracy of submicrons
  - ◆ Haven't shown any wear but if you do it right you can change them
  - ◆ Different types graphene ones - screwing ones
  - ◆ But haven't seen any issue with ATLAS 100-200 times
  - ◆ The question is how many copies of these plates we need
  - ◆ Haven't placed the order with this precision in a while
  - ◆ Need to create prototypes to get them (Berkeley was doing it)

#### UCSC

- Vitaliy - Kirsten shipped out glass chips
  - ◆ Sanghoon got a message from FedEx - it was delivered to PNU, but somewhere else building or office

#### PNU

- Sanghoon
  - ◆ Module and Stave - when the glass dummy is received, will contact the local company, worked together for ALICE, and talk to them
- Ask to get some design files for the modules to discuss the pick and place machine

## General

- Tony - Need to-do list
- The coordinate systems
- Depending on that, get tolerances, quotes, etc
- Order - v3 and v5
- Aug - design ready - signoff
- PED or PREP

## June 2, 2025

Attending: Manoj, Chong, Tony, Blake, Kirsten, Forest, Sanghoon, Kevin,

## UCSC:

We need fiducials for feature findings

Added to the hybrid in the top layer - gold metal dot 200 um

Plus sign - sometimes it doesn't like - bonder program alignment

Vias - drills are not aligned correctly sometimes, so they are not good

Blake will also prefer a circle

Are there any reasons we shouldn't ground the fiducial

If they stay in the right dimensions, no issue with grounding them

The bigger the spacing between eye pads is better

The last chip hybrid is shorter to avoid collision with the flex part of the adjacent module

Need tolerances on the module base plate

Module extrusions are at Argonne but have not been received yet. Kevin will be checking them tomorrow

This will allow us to inspect tolerances

OSU -

Blake thinks Chip starts after the AstroLinx edge

Greg will send out the files

For review -

Evan vandaval

5:45 later time - if Greg will be presenting

We just need feedback from the design in the Box and to schedule the review

Would like Kirsten to sign off

Initial review of readout board - bridge card (given feedback to designer) - approaching submission (put it in the box for review)

## **May 12, 2025**

Attending: Manoj, Greg, Kevin, Tony, Sanghoon, Chong, Bobae, Maria, Forest, Kirsten

Agenda:

Preliminary design of AstroLinx

Status updates

### **OSU**

AstroLinx design is ready for review

Go over the slides and provide your inputs

### **UCSC**

Kirsten received the glass dummies

Need shipping address

Look into the details of what we want, and look at the pickup point

AutoCAD

What format? Kirsten will be emailing it - done

PNU

Waiting for v5 design changes to fit 2cm x 2cm - ask Nicolas

## **Apr 28, 2025**

Attending: Manoj, Chong Kim, Kevin, Tony, maria, Bobae

Agenda:

Preliminary design of AstroLinx

Status updates

PNU -

Dummy chips module production - Possible to fabricate (for all sites) in South Korea.

- Last week, the national conference in South Korea
- I found the design file in the box. Today, I'm sending the design file to the manufacturers.
- Dummy - go with final chip dimensions and give a pad of v5 (for mock-up)

UCSC -

- Glass chips for dicing (1 week for delivery)
- Need addresses to send
- For Stencil, the company needs a diagram for 100  $\mu\text{m}$  bars

- Need bonding diameter
- Make some version of handling tools
- Learn more with the right chip gaps
  - But going with a larger gap gives a more comfortable start
  - Should have a meeting to get the references correct for module assembly.
- Sanghoon - also trying to test another glue (but just make sure radiation hardness is suitable for chips, for AstroPix as well as ALICE) - ITS3 uses ARALDITE-2011
  - Do some tests this year
- UCSC did some glue tests (list of everything available can be shared) (40 min)

After meeting email from Vitaliy (Thanks, Vitaliy)-

Tony mentioned an interest in rad-hard glues. To that effect, I uploaded a couple of presentations to the Box location "[BIC Modules and Staves / Assembly / Glues](#)":

- One is from our studies for ITk Strips. (Note that Epolite and Polaris glues were discontinued since the qualification.)
- Another overview is a CERN seminar from people qualifying for glues for pixel assembly. They generally refer to high-radiation environment, but there is also a reference to older CERN investigation for lower dose.

Is the interest in rad-hard glues due to overlapping work with other project(s)? What I recall for BIC is 1 krad per year (or lifetime), which is rather "small". If this estimate is updated, that would be useful to know.

#### **Apr 14, 2025**

Attending: Manoj, Blake, Kevin, Sanghoon, Vitaliy, Bobae

Agenda:

PED/PREP schedule discussion for the modules team

PED -

With the issues from workshop, it is not possible to have a review by April 22, 2025

Finish design changes this week

It takes a little longer to finalize the design

We kind of have a preproduction turnout plan, things kind of changed with this board, NASA folk to have everything they want

**In the next meeting, we might discuss - making sure we have all the pins we need for v5**

Handling tools - start earlier

- Prototyping
- 6 months

Pick and place machine vs. Handling tools -> decision July 2025

Sanghoon -> For ALICE project

- Packaging company - uses pick and place machine for ALICE module assembly
- Dummy module production with pick and place machine for BIC
- Get position precision, time, and production cost
- ALICE module assembly is ongoing for the first half of the year
- Sanghoon will get back with more information to help with decision
- Potential issue
  - The cure time of glue requires holding the chip in place for the cure time
  - This makes it difficult for auto-assembly
  - It depends on what kind of glue is used, what the cure time is?, whether it fit well with thermal conductivity, radiation hardness
  - The company is building some tooling so that the chip is held in place during cure time using some vacuum tools
  - Sanghoon will find the information and get back

Pre/post protection - wire-bond potting, PCB coating (Parylene vs. conformal coating)

- For wire-bond potting - have experience with Sylgard (Dow Corning Sylgard 184 /186 Silicone?).

Module Assembly (workforce for UCSC)

- For preproduction, the quantity of modules is significant to conflict with ATLAS production at UCSC.
- Don't have the human power to deal with high-quantity module assembly
- After ATLAS production, it will be much better (**3 years from now, i.e. 2028**)
- Planning for half sector (Manoj)
  - 6 layers i.e. 50 staves
  - But we need only four layers, i.e. 28 staves
  - ~350 modules with 3 sites

**Mar 31, 2025**

Attending: Manoj, Tony, Blake, Kevin, Vitaliy, Forest, Kirsten

Agenda:

Questions from Forest (will redirect to Steven and Blake)

What is the reasoning behind choosing this connector?

Do we have any experience using this connector?

How many times the connectors can be used?

OSU

- Presentation during In-Person meeting
- Design is ready - review internally
- Work on updates after that
- Discussion about possible signals needed

Branches for each of the module  
Got the stack up from a vendor  
Rigid-flex - trying to use materials with minimum loss

Tony

Assuming for connector losses?

Not considered any loss for connector

In the past seen connectors with loss - 3 dB/connector

Kirsten

- Need pickup area - 4-5 mm<sup>2</sup> at several places.

Tony

Copper balancing for glue balance.

The bottom layer is mainly copper-filled - Most likely ground (some routing there, chip select, and power)

Transmission frequency - 20MHz (highest Blake could find, everything was 20MHz, something with 3.125 ns)

Howard Johnson reference - 2 m with 20 MHz will be dominated by LC transmission (Vitaly)

- Rise time and fall time will be affected
- How fast can you get an eye diagram

Fabrication needs to be decided - it depends on the funds.

The flex region needs some space for bending radius - the jumper is another option, but it will double up the losses connector.

UCSC

Kirsten - find the glass vendor.

Brainstorming - relevant aspect of handling and wirbondings

### **Mar 17, 2025**

Attending: Manoj, Bobae, Kevin, Tony, Forest,

Agenda,

Module Design

Module Stave design ideas

Astrolinx

Dimensions and location of PCB

Assembly for ALICE?

Wire bonds are good with 45 deg angle

Small mockup of pad geometry - to see if wire bond is possible

Data connectors provide datasheet

Forest sent 45 deg clearance requirements for wire bonding (from lower to higher height)

V3 and v5 chips are different sizes from the final chip; v6

Ask for wirebond plan to OSU

Carriers

UCSC -

Waiting on drawings

Tooling will include -

Module assembly

Bonder (similar)

Pickup

Do we need tools to move the module?

Designing holders - write down what we want to do. It is more complicated than something attached to the module (it comes off and on). Think about the purpose of each tool and figure out extra features

Think about permanent deformation from the tools.

Write down purposes for tools.. numbers, names...

Questions from Forest (will redirect to Steven and Blake)

What is the reasoning behind choosing this connector?

Do we have any experience using this connector?

How many times the connectors can be used?

**Mar 3, 2025**

**Updates at Argonne**

- Module design
- Wirebond discussion
- SPI pad wire bonds

Wire-bond plan - request to OSU

HV bonds - not bad (300-400V)

Wirebond crossing

SPI staircase needs the other way round - talk to Nicolas

HV away from SPI

Chip-to-chip case minimum case

~1 mm

OSU

Pads for the first chip are routed  
Greg last week updated the design  
Flex region four-layer board  
Rigid region eight-layer board  
Power regulators for all four voltages for v3  
Select solder bridges -  
Connector on the bottom - upstream connector  
The connector on the PCB is a downstream connector  
Used voltage regulators from 9chip pcb  
Voltage drop along the stave  
516 mV drop across the stave  
6V is good but can we do 9V?  
    5V doesn't seem feasible (5V may work - need verification!)  
    - Power dissipation with 9V is better for stave  
Chip select from 12 pin through connector and 1 pin to chip - need soldering  
USCS requested wirebond plan with chip overlap  
OSU uses Altium  
Connector move - inside to align flex part

UCSC

Dummy glass - no response from past company so exploring other options  
No grad-student or postdoc to work on DAQ

**Feb 17, 2025**

**UCSC updates -**

Ordered some parts of fancy aluminum for toolings.

Need PCB material details for glue studies - module assembly  
Blake

- trouble with vendors to get the right stack up
- they gave the recommended stack-up but not good
- signal integrity is not good
- The solder mask is not going to change much

not high requirements - mechanical stability, glue bond,  
Blake can provide vendor contact

Vitaliy needs to go back to UCSC technicians and check

Glass dummies

500 - suitable option

550 um thickness

/pm 15 um getting quote

1.66mm height wirebondings

- UCSC did some testing like this in the past

- Bond ability to check the length of wire bond
- Test horizontal length and vertical studies at UCSC
- Vitaliy said they can do it

## OSU -

Routing the traces and pads

1.2V + 1.8V vssa-vdda can be tied together

18V supply

Which pads are needed or not needed - provide the list of pads to Blake (For Manoj)

1.6 mm in height, the pads are vertical - wire bond strength will be weak. The angle is mechanically weak

The angle of approach should not be 90 deg but less for wire bonding

For vminuspix voltage of 0.7 V - a voltage divider can be used

Comment on Schedule -

Bootstrapping timeline

## Feb 3, 2025

Timeline and structure

PED

BIC workshop - most likely early Apr

Updates at Argonne -

- Progress from Nov - Dummy Module and PCB test module 🎉
- Kevin sent the first CAD iterations with a step file from Blake
- Next steps
  - Dummy mockup
  - Testing of PCB board
- Blake
  - checked file from Kevin
  - Rework and send it back to him

Updates at PNU -

- As BIC astropix side - more testing for wafer testing
- ALICE - Korea involved in module production
  - The module structure is a bit different from the ALICE tracker
  - Working with company
  - Dummy module
  - Position procedures
  - Successfully produced dummy modules
  - The next meeting will shows
- For AstroPix modules - provide design files
  - Can start co-ordinate with company
  - ALICE chip is thicker and smaller

- The precision requirement for Alice is 10s microns
- For BIC, it is 50-100 microns

#### Updates at UCSC

- A bit futuristic -
  - Received prototype boards and chips
  - Can do it by hand
  - Thinking about making jigs, much less handy and more assembly line
  - Borrowing procedure from other projects
  - Glue - Atom Adhesive F112
    - It will be good to share datasheet
  - Glass chips with the right size and thickness
    - UCSC does have vender contacts
    - What to know about glue thickness
  - Solder resists going to be on the board
  - The nice thing about Flase glue - Cure time of 3-4 hrs +
    - Can use glue robot, radiation hard
  - What solder resists on the PCB?
    - Blake -
      - Most likely, the solder mask
      - That section of the board will be rigid
      - If you need different material, it can worked out
      - Just need to knowthe material, and we can do studies (Tony)
      - Blake will know it this week (good point to start)

#### Updates at OSU

- Greg is a lead designer
- Have slides and have a few questions
- Design ideas that will work
- Constraint
  - Stack up that we can use have some flexibility in the region with overlap
- Slides
  - The entire board is 15.52 mm
  - Mockup with material and stack up
    - ~1.6 mm rigid and 300 um flex
  - Designed Half of the board for mock-up
  - 4 data lines, GND is not shown
  - Low and High voltage lines on the left side of slide 7
  - Mock-up with thick PCB of 1.6
  - Budget for PCB fabrication
    - Working on contract for actual board themself
    - If there is material money

#### PED heads up for next meeting -

- We have timeline
- But we need to know how much we can achieve and how much delay we expect

- Think about when we can finish up the stuff and give a new target according to the new timeline
- More detailed discussion on who is doing what

August 26, 2024

Outline:

Mechanical Design of the Module - Kevin

Flex Design

Discussion of the connector on flex

Connector width and height

Wide Flex on module and width can be narrower off the module

Longer and narrower connector

How to fit the modules

I/O pin requirements.

Minutes:

AI plate

- HV bias - Thin layer of Kapton (Vitaliy)
- Thermal conduction, mounting on tray, alignment, wire bonding support,
- we haven't finalized the concept for the Tray (Sylvester)
- Steven - get rid of the AI block and mount the chip directly on the Tray
- Let the PCB be your rigid support - Steven (anyway there is a vertical size constraint).
- Optimization - assembly - Steven
  - That means we are assembling a full tray
  - Stability of full Tray (Vitaliy, Tony)
  - Vitaliy - 1 mil thick insulating layer is sufficient
  - Module PCB
  - Mount 9 chip on the module - test it
  - build N modules and test them at a time and then assemble - Vitaliy

Flex Connector

- Why the range of pins 57- 87 (Steven)
- Need more gnd pins in between
- Impedance mismatch (Blake)

Steven Slides

Communication protocols -

I2C -

Common interface for microcontrollers

2-wire interface -> bi-direction data and clock

Speed 100kbps to 3.4 Mbps over 4 meters (increase it if uses directions differential repeaters)

Single line - no impedance control, not much termination, single ended

Only talks to one device at a time (like SPI)

But can have 128 devices on the same bus

Block diagram for I2C bus (slide 3)

- controller, devices, branching structure (pullup resistors)
- It cannot be implemented on PCB precisely as shown in the block diagram; it is more complicated to make tracks on PCB as it introduces issues
- Special techniques to use the multidrop data lines
- Controller send the messages

SPI

- 3 or 4 wires
- higher speed 1 - 20 Mbps
- 10 meters and if convert it to differential bus it can go upto 100 meters
- one device on the bus at a time - separate clock line,
- shared bus
- - need active low signal for every device - chip select
- 
- This is a MultiNode parallel method
  - Simulation required - multi-drop distribution
  -
- Daisy chain (not necessarily exactly the same as for AstroPix, but the basic logic is somewhat similar)

Single ended to differential needs differetial driver chips (slide 8)

Chip select - Dc line - very slow

Chip select - how does it work? Can it be serialized?

- If we do not have enough chip select lines, this system might not work
- Multiple modules (12) come to the end of the Tray card
  - If we use single-ended transmission line the design structure is achievable (slide 11)
  - Should do that
  - At least 16 lines to have one stave single-ended
  - Install some multiplexers
    - And use I2C
- Multiplexer for chip selected needs to be single-ended
- We can look at multiplexer speed - hits in multiple modules
- Are we using interrupt?
- Decisions we make now will have an impact later
- Conservative now for the module design on flex PCB - and in future make some compromise...
- Vitaliy
  - Differential - way too many lines
  - Single-ended - we might have cross-talk
    - Can mitigate cross talk with good pcb design (put grounds)
    - Can put GND between pins (also true for differential) - Steven
  - Feasibility (way to many lines)

- Width of the pins on connectors
- Difficult to assess theoretically
  - Rule of thumb - differential work better
  - Differential for clock and data and single-ended for chip select
- Cross talk and noise induced by the lines (how much space between lines and chips)
- Not constraint on space, drive with constraint on interfaces (connectors)
- Smatech has ground blades instead of gnd pins
- Considering 20 lines are still a lot
- On the order of 30 pins, can consider
- I did not even think about custom connectors
  - 3-4 years of development
  - Commercial solutions
  - Which one might work for these operations
  - substantially smaller than LPAM connectors
- The impedance of the connector must be very low if it is mounted on silicon - mate/demate them.
- Hard to solder, hard to mate - demate
- Need serious structure underneath the connector to support demating
  - Better smaller options are available
  - Change the design of vias, change glue, etc.
- The mating force on the flex is different depending on the gender of the connector.
- From experience, the male connector has a lot of force.

Reach out to KIT with questions related to the Chip interface.

Steven will look into more connector options (significantly smaller)

Revisit the Pinouts for the End-Of-Tray card - - Module interface.

Kapton (insulating layer) in between AstroPix Back (HV) and AI-plate

Steven - get rid of module AI base plate on mount chips directly on Tray

To have a module reworkable, test a system at Module level

Optimization - test stability may not be ideal, if some modules are bad they can be replaced easily

Questions:

1. Chip select single line is connected in series for different chips in daisy chain. Each chip needs to get the active low to send the data - how does this system work? Can it be serialized within the module (Manoj - It goes low for all chips in the daisy chain)? How do we know which chip needs to go active low when data arrives?
2. Chip select needs to be single ended instead of differential - which will be slower but should work
3. Do we need Interrupt lines? Without interrupt you can hold these things even 20 Mbytes. If we have interrupt line then we are back to 30 pins datalines
4. Differential for clk and data, single ended single for Chip select?

Answers:

1. Chip-select: It is daisy-chained on the modules (for 9 chips). The chip-select signal is propagated/buffered from chip to chip. So if we set the chip select as active-low, other chips in the chain are also set to active-low. So, we can put the entire module as active-low and not an individual chip. The broadcast commands can be sent to the individual chips using their ChipID. The chip responds, and records hit independently of chip-select status, and the chip-select active-low is only needed for the SPI communication.
2. Interrupt: The data can be read out without connecting the interrupt lines. The interrupt line is a status output signal showing which module you want to read out and for how long. Of course, one can apply a round-robin-based readout scheme and read out until you get something like 9\*2 IDLE Bytes and then hop to the next module. The chip can generally store one hit for every pixel because each pixel has one hit buffer. Additionally, there is a small readout fifo that can store 8 hits. If this fifo is full, the hitbuffer readout stops. Now, if a pixel gets a hit B and the hitbuffer already stores a hit A, then hit B will be lost.
3. SPI bus: The status of the SPI FIFOs for incoming and outgoing data in the chain, as well as the readout fifo, is considered in the interrupt logic. Interrupt still has to connect for all chips even if we only want to look at the SPI chain FIFOs because one chip does not know if the other chips have something in their SPI FIFOs.
4. Differential vs. single-ended: AstroPix currently only uses the single-ended or differential interface. Nevertheless, as a workaround, we can use the differential interface for 4 SPI lines (1 CLK, 1 MOSI, 2 MISO) and connect SPI\_CSN\_N to VDD/2 and drive SPI\_CSN\_P as a single-ended 1.8V CMOS Signal. On the other hand, there will be a pad "use\_spi\_diff," which allows either the single-ended interface or the differential interface for all 5 SPI buses.

2 MISO needs to be differential

It needs to be tested.

Other SPI line's differential N pin needs to be connected to half the supply voltage (VDD/2)