A

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S5 (R, S) / S3 (PT) (R, S) Examination December 2023 (2019 Scheme)

Course Code: ECT 301

Course Name: LINEAR INTEGRATED CIRCUITS

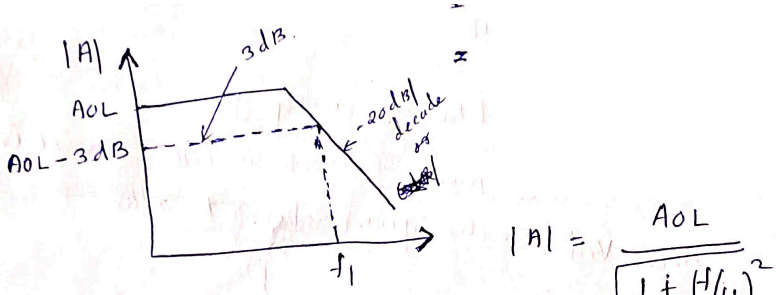
Max. Marks: 100 Duration: 3 Hours

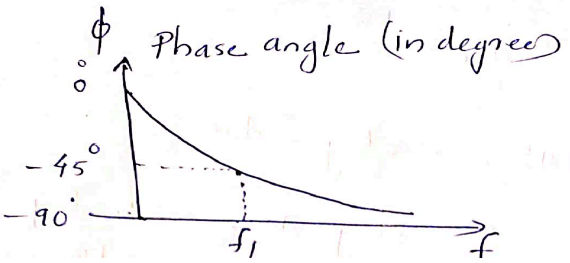
PART A

(Answer all questions; each question carries 3 marks) Marks

1 Discuss the frequency response curve of an operational amplifier. 3

Frequency Response Curve





$$\phi = -\tan^{-1}\left(\frac{f}{f_1}\right)$$

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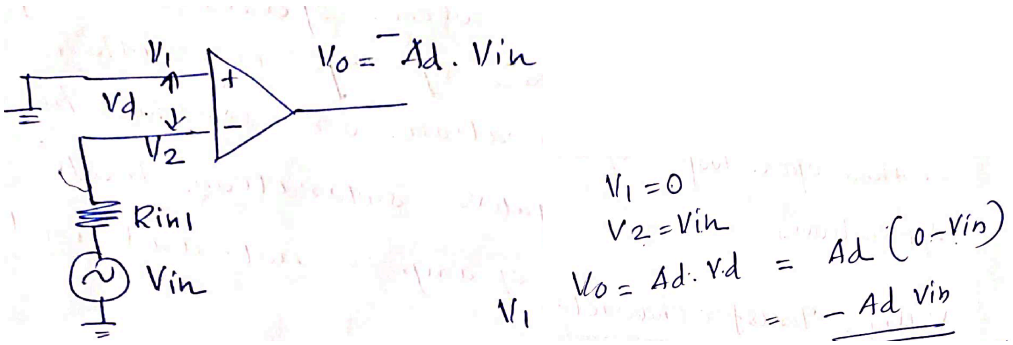
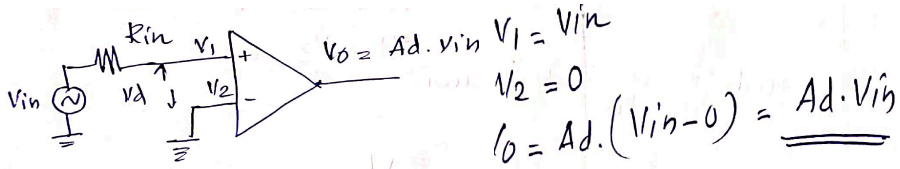
2 Differentiate between the open loop configurations of inverting and non-inverting amplifiers. 3

1.5 marks for inverting and 1.5 marks for non inverting configuration

inverting



non inverting



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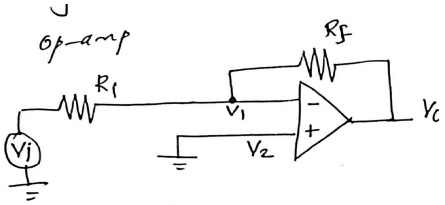
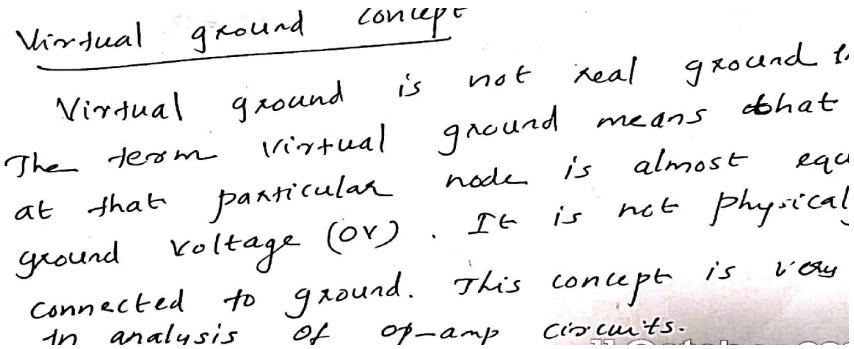
3 Discuss the concept of virtual ground in inverting amplifiers. 3

1 mark for circuit diagram+2 marks for explanation




Virtual ground concept

Virtual ground is not real ground i.
The term virtual ground means that
at that particular node is almost equ
ground voltage (0V). It is not physical
connected to ground. This concept is very
in analysis of op-amp circuits.

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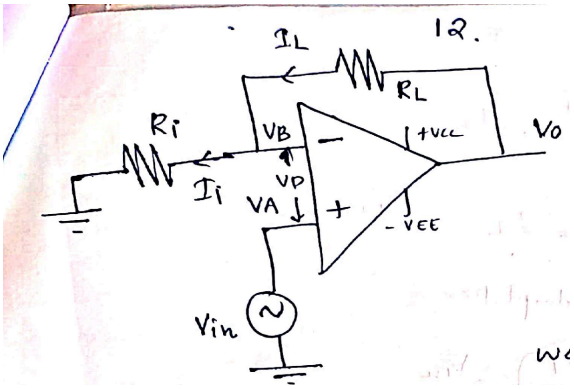
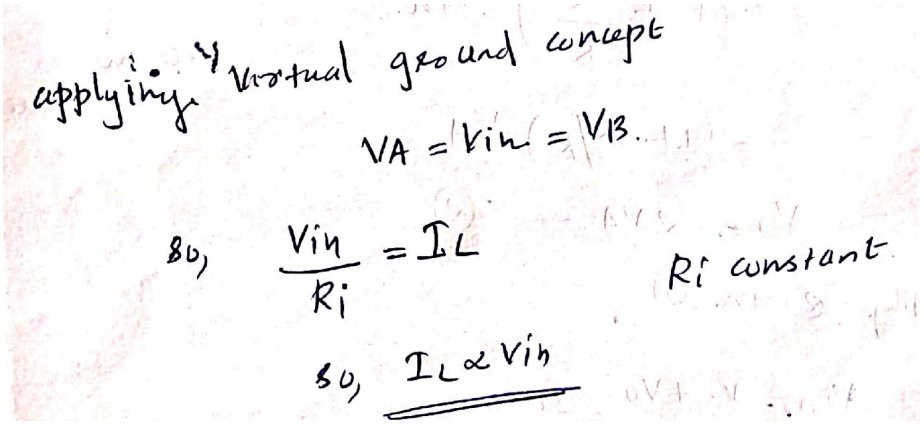
4 Explain the working of voltage to current converter with floating load. 3

1 mark for diagram +2 marks for equations





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5 Design a notch filter to eliminate power supply hum (50Hz) 3

Let C=0.1μF

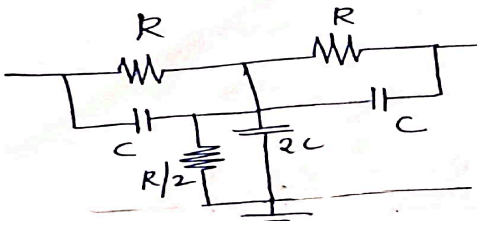
$f_o=\frac{1}{2\pi\sqrt{6}RC}$;

R=1.083 K

To prevent the RC network from loading the amplifier it is selected such R1 >10R.

Letting R=1 K, R1=10K

$R_F=29R_1$;$R_{F=}$290K



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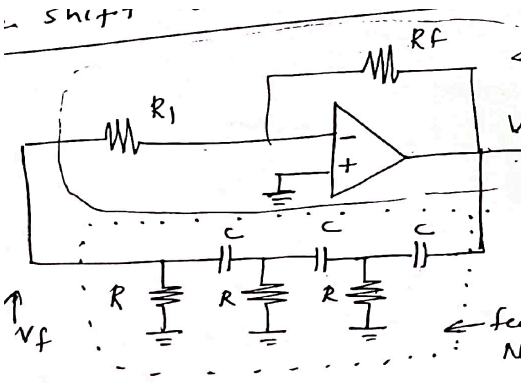
6 Design a RC Phase Shift Oscillator for a frequency of oscillation of 600 Hz using µA 741. 3



Let C=0.1µF

$f_o=\frac{1}{2\pi\sqrt{6}RC}$;

R=1.083 K

To prevent the RC network from loading the amplifier it is selected such R1 >10R.

Letting R=1 K, R1=10K

$R_F=29R_1$;$R_{F=}$290K

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7 In a VCO. if input signal frequency is 10 kHz, free running frequency is 14kHz, voltage to frequency conversion factor is 2kHz/V, find the change in the dc control voltage, during lock. 3

Frequency Shift, Δf=14kHz-10kHz=4kHz

$$\Delta V = \frac{\Delta f}{V \text{ to } F \text{ Conversion Factor}} = 2\text{V}$$

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8 Explain how PLL can be used as a frequency multiplier. 3

2 mark for Diagram+1 mark for explanation.

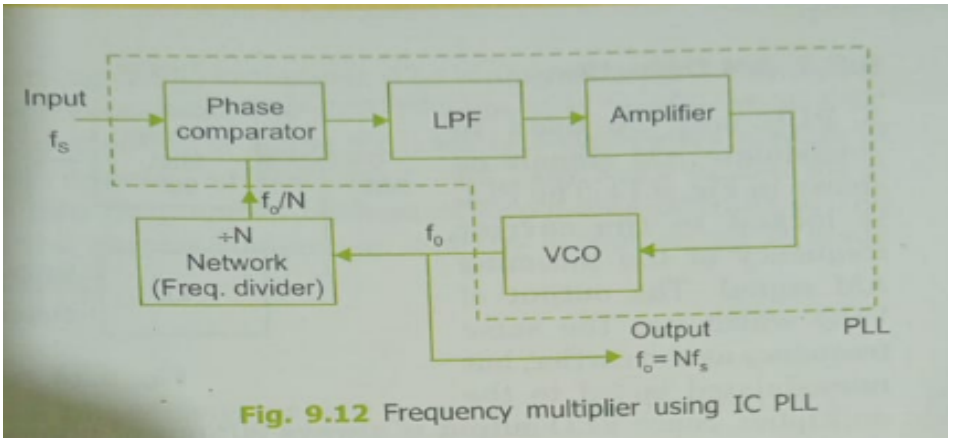

Fig. 9.12 Frequency multiplier using IC PLL

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9 Find the resolution and dynamic range of a digital to analog converter, if the maximum peak to peak output voltage is 5V and the input signal is a 10 bit word.

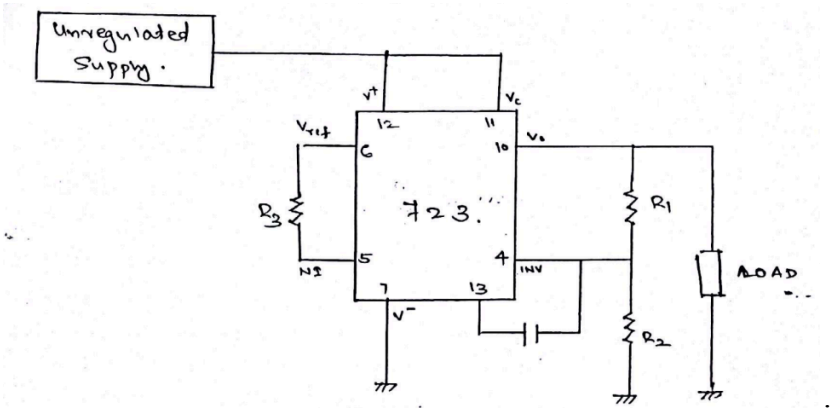
$$\text{Step size}=\frac{5V}{1024}=4.88\text{mV}$$

$$Dynamic\ Range = \frac{5V}{4.88mV}=1024$$

$$\text{Dynamic Range in dB}=60\text{dB}$$

10 Explain how 723 IC can be used as a high voltage regulator. Give the equation for output voltage. 3

2 marks for circuit diagram+1 mark for equation



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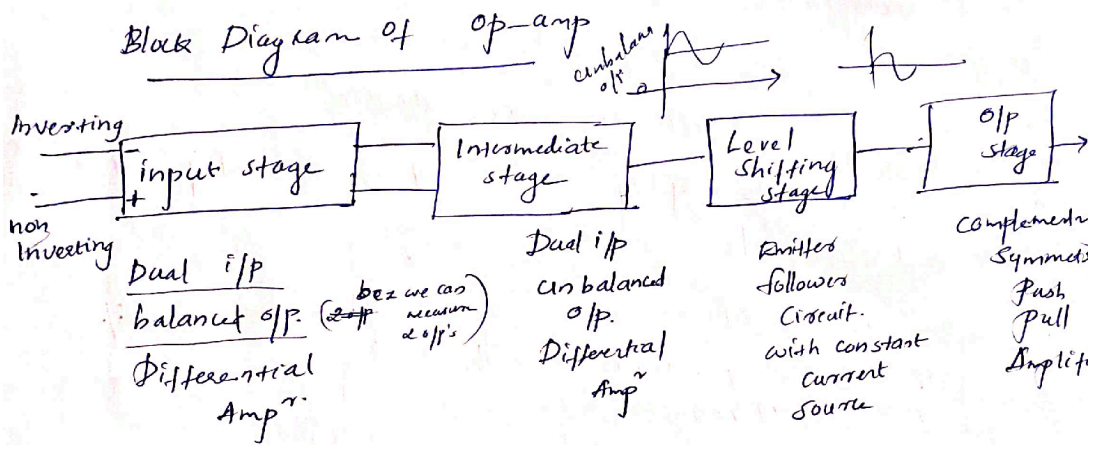
PART B

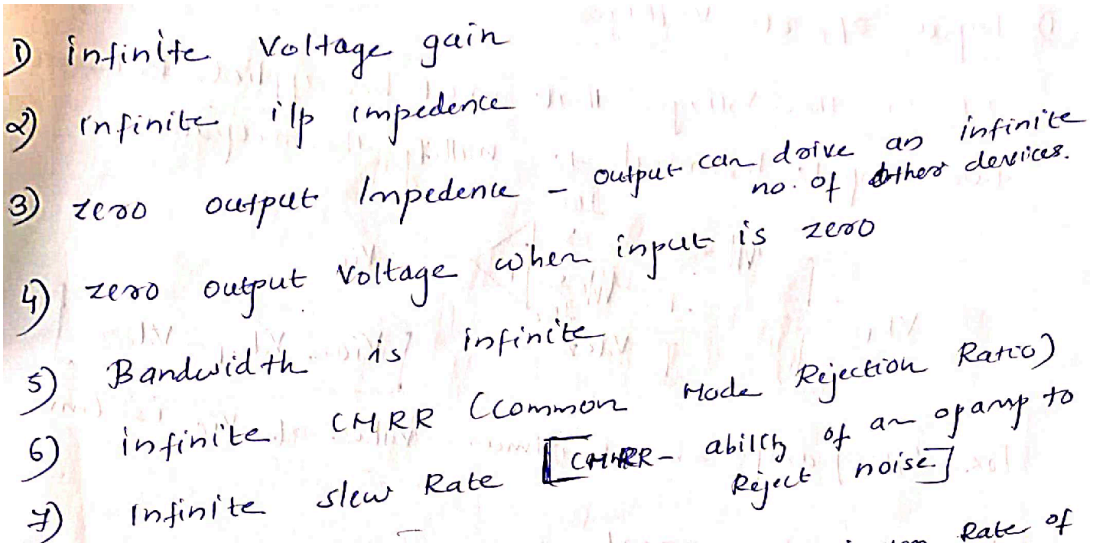
(Answer one full question from each module, each question carries 14 marks)

Module -1

11 a) Explain the block diagram of an operational amplifier. List out any four ideal op amp characteristics. 7

2 mark for block diagram+ 1 marks for explanation+4 marks for characteristics.





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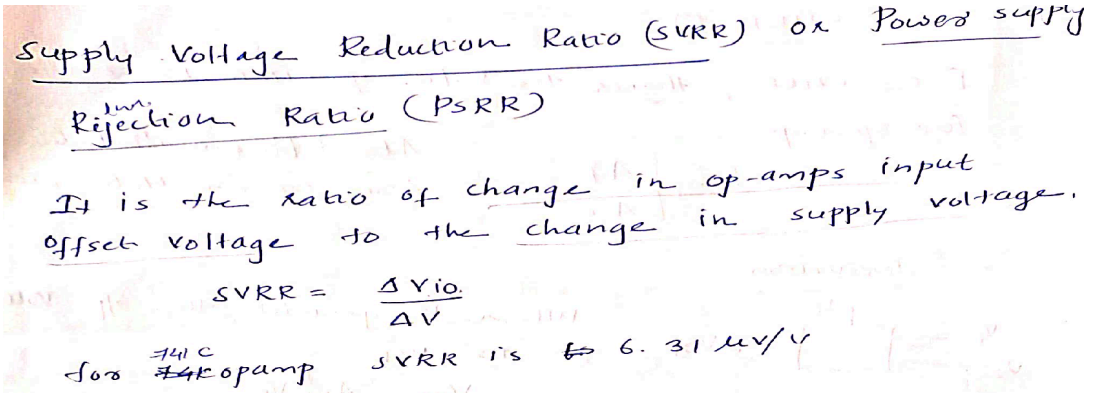
bb) Define a) Power Supply Rejection Ratio b) Input Bias Current of an op amp. Draw the equivalent circuit of an opamp. 7

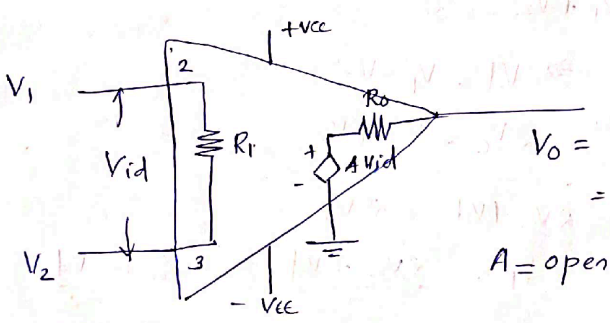
2 mark for Power Supply Rejection Ratio and 2 marks for Input Bias Current and 3 marks for equivalent circuit



input bias current I_B

I_B is the Average of the current flow in t
Inverting and non Inverting input terminals of the
op-amp $I_B = \frac{I_{B1} + I_{B2}}{2}$ maximum Value for
741C is 500nA

Equivalent circuit diagram of op-amp



$V_o = A \cdot V_{id}$
$= A(V_1 - V_2)$
A = open loop gain

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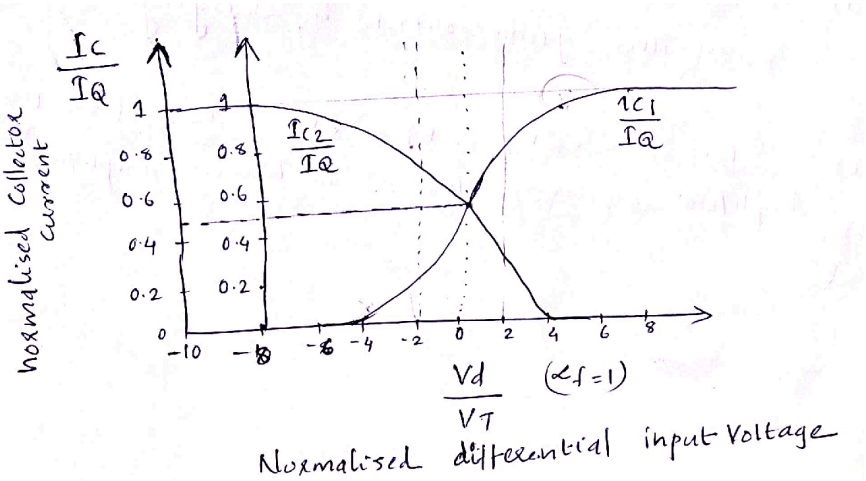
12 a) Discuss the transfer characteristics of differential amplifiers. 7

2 marks for graph+3 marks for equations+2 marks for explanations from the graph.



$$i_{C1} = \frac{\alpha_f I_Q}{1 + e^{-V_d/V_T}}$$

$$i_{C2} = \frac{\alpha_f I_Q}{1 + e^{+V_d/V_T}}$$

a) for $V_d > 4V_T$ $\quad i_{C1} = \alpha_f I_Q$ and i_C

$$V_{O1} = V_{CC} - \alpha_f I_Q R_C$$

$$V_{O2} = V_{CC}$$

By proper value of R_C, V_{O1} can be made or

b) for $V_d < -4V_T$

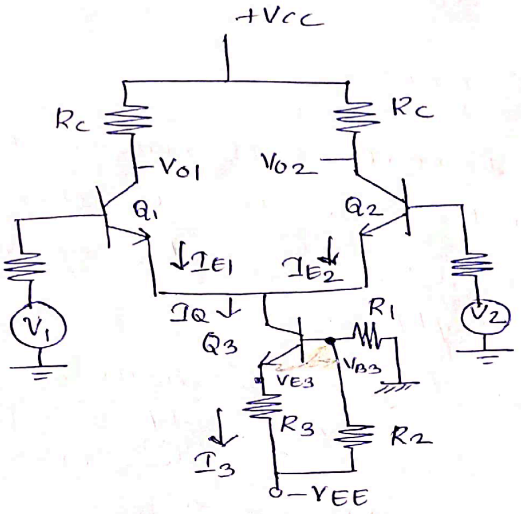
$$i_{C1} = 0, \qquad i_{C2} = 4I_Q$$

$$V_{O1} = V_{CC}$$

V_{O2} is small

. $4V_T < V_d < -4V_T$, This can be operated as switch.

b) Explain how differential amplifier using constant current bias improves CMRR.
2 marks for circuit diagram+2.5 marks for equations +2.5marks for explanation. 7



we have, $I_3 = \frac{V_{E3} - (-V_{EE})}{R_3}$

$= \frac{V_{E3} + V_{EE}}{R_3}$ ——— (1)

$V_{B3} = -V_{EE} \cdot \frac{R_1}{R_1 + R_2}$ ——— (2)

$V_{BE3} = V_{B3} - V_{E3}$ ——— (3)

$V_{BE3} = -V_{EE} \cdot \frac{R_1}{R_1+R_2} - V_{E3}$

$V_{E3} = -V_{EE} \cdot \frac{R_1}{R_1+R_2} - V_{BE3}$.

Sub. V_{E3} in (1)

$I_3 = \frac{-V_{EE} \cdot \frac{R_1}{R_1+R_2} - V_{BE3} + V_{EE}}{R_3}$ ——— (4)

$I_Q \approx I_3$

$I_Q = I_{E1} + I_{E2}$

if $I_{E1} \approx I_{E2}$

$I_Q = 2 I_{E1}$

Sub. in (4)

$2 I_{E1} = \frac{-V_{EE} \frac{R_1}{R_1+R_2} - V_{BE3} + V_{EE}}{R_3}$

$I_{E1} = \frac{-V_{EE} \frac{R_1}{R_1+R_2} - V_{BE3} + V_{EE}}{2R_3}$

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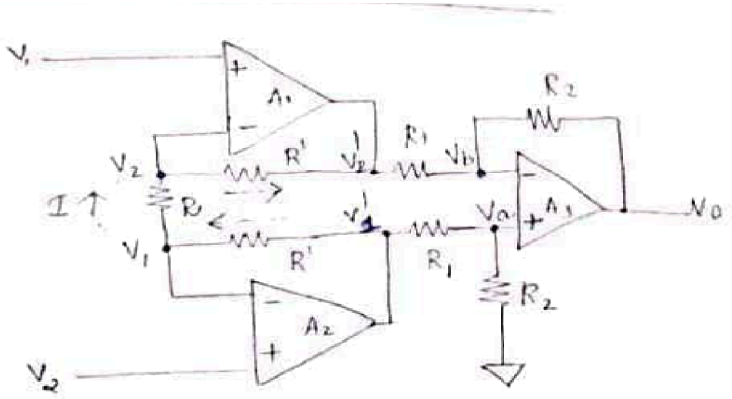
Module -2

13 a) Derive the equation for the output voltage for an instrumentation amplifier using 3 op amps. 7

2 marks for circuit diagram and 5 marks for equation derivation



according to superposition theorem,

$V_o = V_{oa} + V_{ob}$.

V_{ob} – V_o due to V_b. $\quad V_{ob} = -\frac{R_2}{R_1} V_2'$

$$V_{oa} = \left[1 + \frac{R_2}{R_1}\right]\left[\frac{V_1' R_2}{R_1 + R_2}\right]$$

$$\therefore V_o = V_{oa} + V_{ob}$$

$$= \left[1 + \frac{R_2}{R_1}\right]\left[\frac{V_1' R_2}{R_1 + R_2}\right] - \frac{R_2 V_2'}{R_1}$$

$$= V_1' \frac{R_2}{R_1} - \frac{R_2}{R_1} V_2'$$

$$V_o = \frac{R_2}{R_1}\left[V_1' - V_2'\right] \quad \text{——①}$$

If $V_1 \neq V_2$ then current flowing in resist

$V_1' = IR' + V_1$ } in ① $\qquad I = \frac{V_1 - V_2}{R}$

$V_2' = -IR' + V_2$

$$V_o = \frac{R_2}{R_1}\left[IR' + V_1 - \left[-IR' + V_2\right]\right]$$

$$= \frac{R_2}{R_1}\left[\left[\frac{V_1 - V_2}{R}\right]R' + V_1 + \left(\frac{V_1 - V_2}{R}\right)R' - \right.$$

$$V_o = \frac{R_2}{R_1}\left[\frac{2(V_1 - V_2)}{R} R' + V_1 - V_2\right]$$

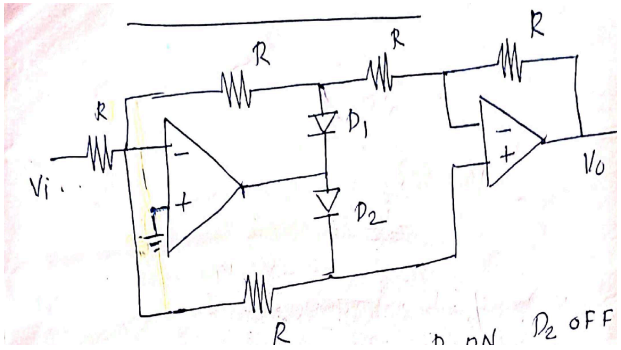
$$V_o = \frac{R_2}{R_1}\left[\frac{2R'}{R} + 1\right](V_1 - V_2)$$

Gain of instrumentation amplifier,

$$\frac{V_o}{V_1 - V_2} = \frac{R_2}{R_1}\left[\frac{2R'}{R} + 1\right]$$

b) Explain the working of full wave precision rectifier. 7

2 marks for circuit diagram+2.5 marks each for explanation during positive half cycle and negative half cycle.



$$\frac{V_i}{R} + \frac{V}{R} + \frac{V}{2R} = 0$$

$$-\frac{V_i}{R} = \frac{3V}{2R}$$

$$V = \frac{-2V_i}{3}$$

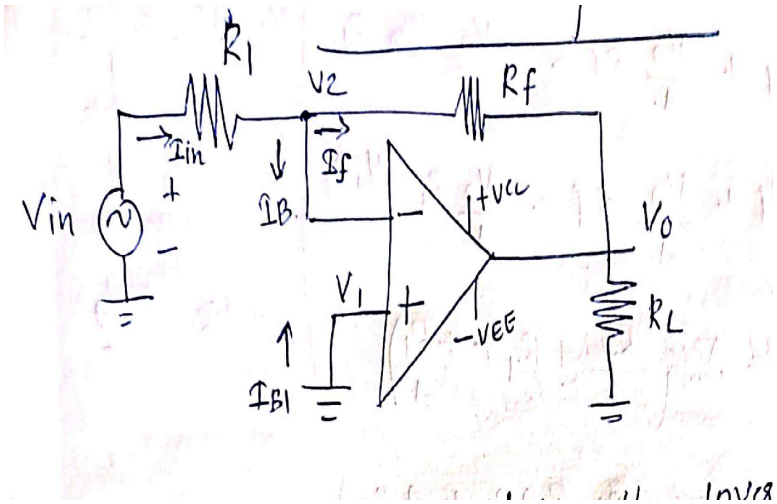
$$\Rightarrow V_o = 3/2 \cdot V = \frac{3}{2} \cdot \frac{-2}{3} \cdot V_i$$

$$\therefore \boxed{V_o = -V_i}$$

from negative input ($-V_i$) Output is positive

14 a) Derive the equation for closed loop voltage gain, input and output resistance of voltage shunt feedback amplifier. 7

1 mark for circuit diagram+2 marks for derivation of voltage gain+2 marks for derivation of input resistance+2 marks for derivation of output resistance



$$A_f = \frac{kA}{1+AB}$$

$k = Rf/R1+R1$

$B = \beta$

if $AB >> 1$

$1 + AB = AB$

$$A_f = \frac{-k \cdot A}{AB} = \frac{-k}{B} = \frac{\frac{-Rf}{R1+Rf}}{\frac{R1}{R1+Rf}} = -Rf/R1$$

Since R_i and A are large

$$\frac{R_F}{1+A} \parallel R_i \approx 0$$

$$R_{if} = R_i \quad \text{(ideal)}$$

$$R_{of} = \frac{R_o}{1 + AB}$$

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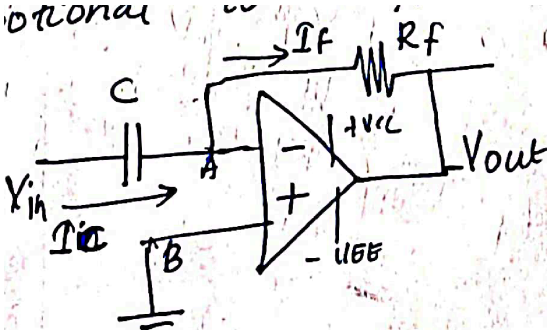
b) Derive the equation for output voltage for a differentiator. Explain the frequency response of differentiator. 7

2 mark for circuit diagram+2 marks for derivation +3 marks for frequency response.



Apply KCL at node A

$$I_{in} = I_f$$

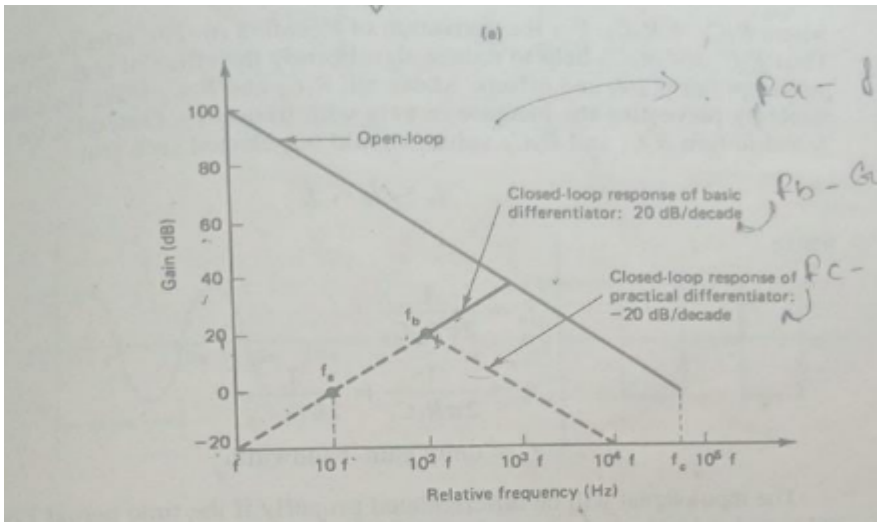
$$C \cdot \frac{d}{dt} V_{in} = \frac{0 - V_{out}}{R_f}$$

$$V_{out} = -R_f \cdot C \frac{d}{dt} V_{in}$$

$i = \frac{dQ}{dt}$

$Q = CV$

$i = d$



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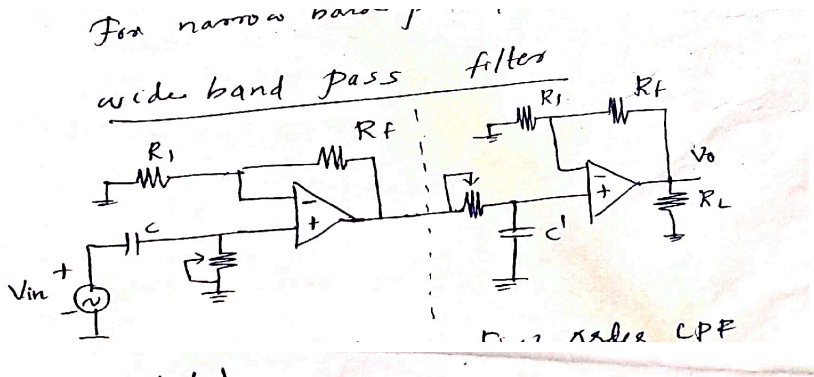
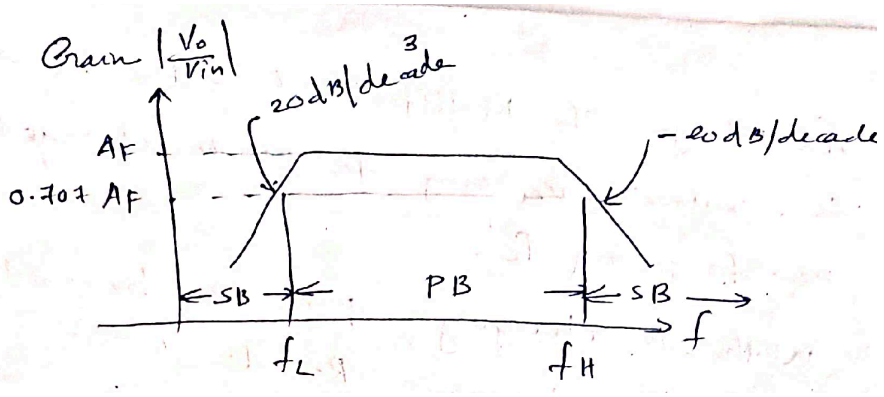
Module -3

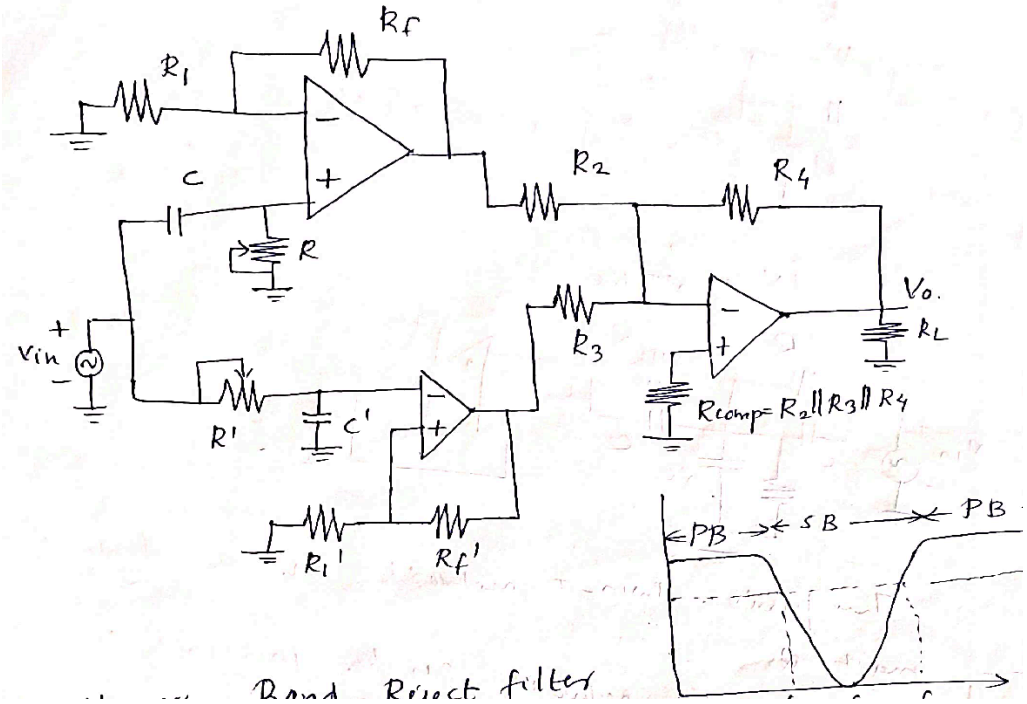
15 a) Illustrate how the following filters can be implemented using opamp. Draw their frequency response. 7

1) Band Pass Filter 2)Band Reject Filter.

2.5 marks each can be given if the circuit diagram is drawn. 1 mark each can be given for frequency response (3.5*2)







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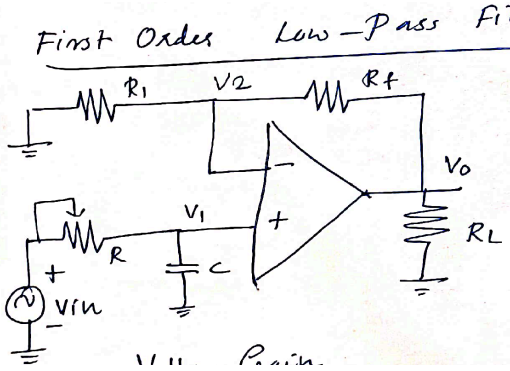
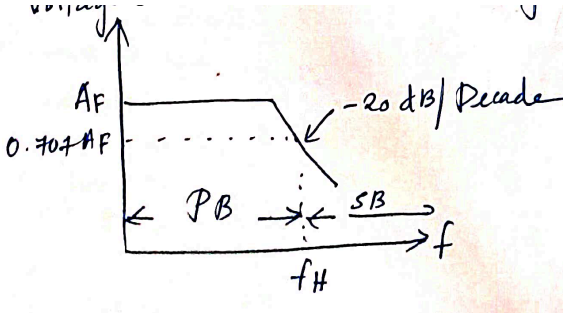
b) Derive the equation for voltage gain for first order low pass filter. Using the gain magnitude equation illustrate the variation of gain with respect to frequency. What is frequency scaling? 7

2 marks for circuit diagram+ 2 marks for derivation of voltage gain +2 marks for variation of gain with respect to frequency+1 mark for frequency scaling

First Order Low-Pass Filter





$$\text{magnitude } \left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^2}}$$

$$\text{Phase } \phi = 0 - \tan^{-1}(f/f_H)$$

Frequency scaling is the process of converting original cut off frequency to a new frequency

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16 a) Explain the working of a monostable multivibrator using 741. Derive the equation for pulse width. 7

2 marks for circuit diagram+2 marks for explanation+3 marks for derivation of pulse width.

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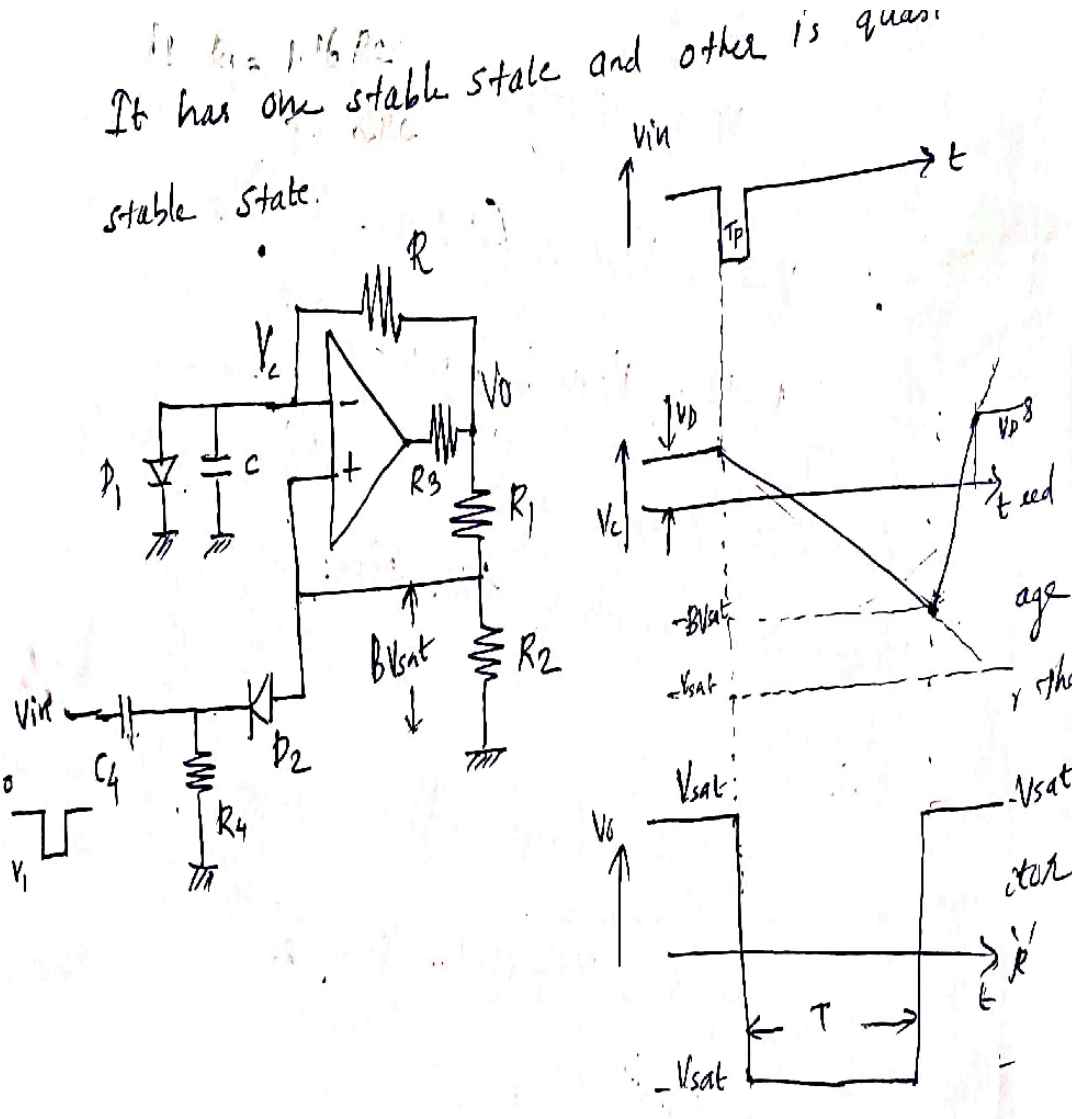
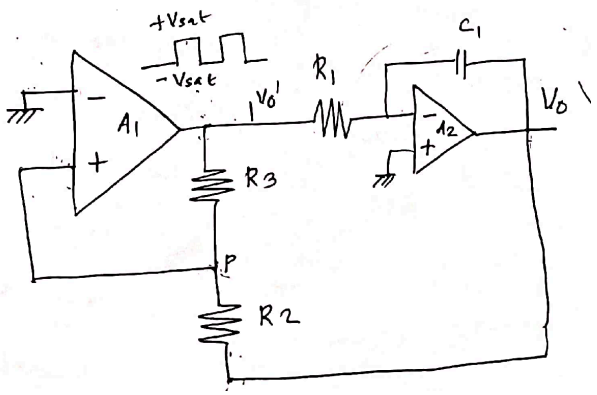
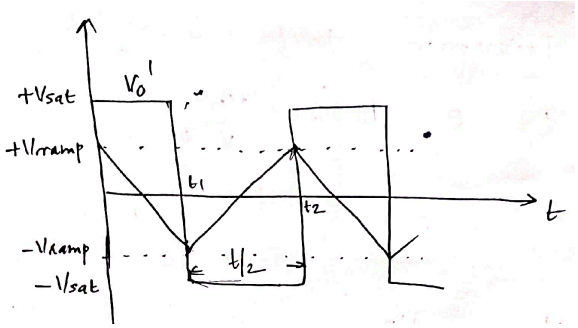


$$T = 0.69\ RC$$

b) Explain the working of triangular wave generator. Derive the equation for frequency of oscillation. 7

2 marks for diagram+2 marks for explanation+3 marks for derivation of frequency of oscillation.





During the time when the output of A1 is at -Vsat, the output of A2 increases in the pos direction.

At instant t=t2, the voltage at point 'P' bec just above 0V, there by switching the output A1 from -Vsat to +Vsat. This cycle repea and generates the triangular waveform.

o/p of Integrator

$$V_0 = \frac{-1}{RC}\int v_i\,dt$$

$$V_0(p\text{-}p) = -\frac{1}{R_1C_1}\int_{T/2}(-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\int_0 dt$$

$$= \frac{V_{sat}}{R_1C_1}(T/2-0)$$

$$V_0(p\text{-}p) = \frac{V_{sat}}{R_1C_1}\,T/2$$

$$\frac{2R_2}{R_3}V_{sat} = \frac{V_{sat}}{R_1C_1}\cdot\frac{T}{2}$$ from eqn (3)

$$\frac{2R_2}{R_3} = \frac{T}{2R_1C_1}$$

$$\boxed{T = \frac{4R_1R_2C_1}{R_3}}$$

$$f_0 = \frac{R_3}{4R_1R_2C_1}$$

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Module -4

17 a) Explain the astable operation of 555 timer I.C. Derive the equation for frequency of oscillation. 7

2 marks for functional block diagram+2 marks for explanation+3 marks for derivation of frequency of oscillation

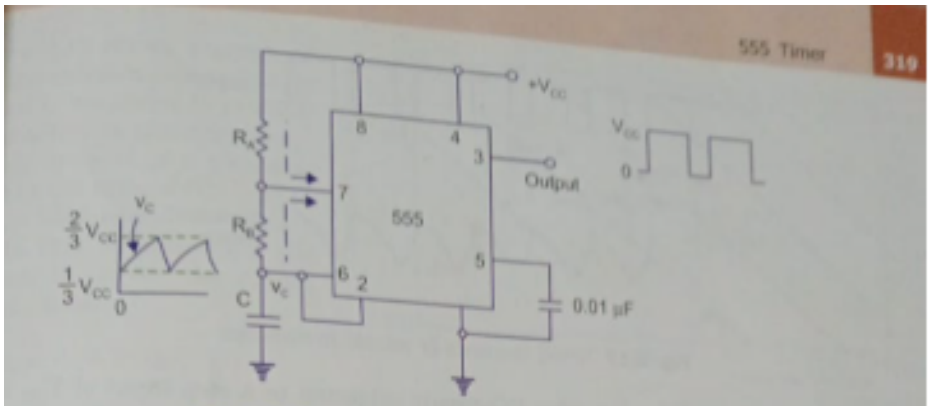


Fig. 8.15 Astable multivibrator using 555 timer

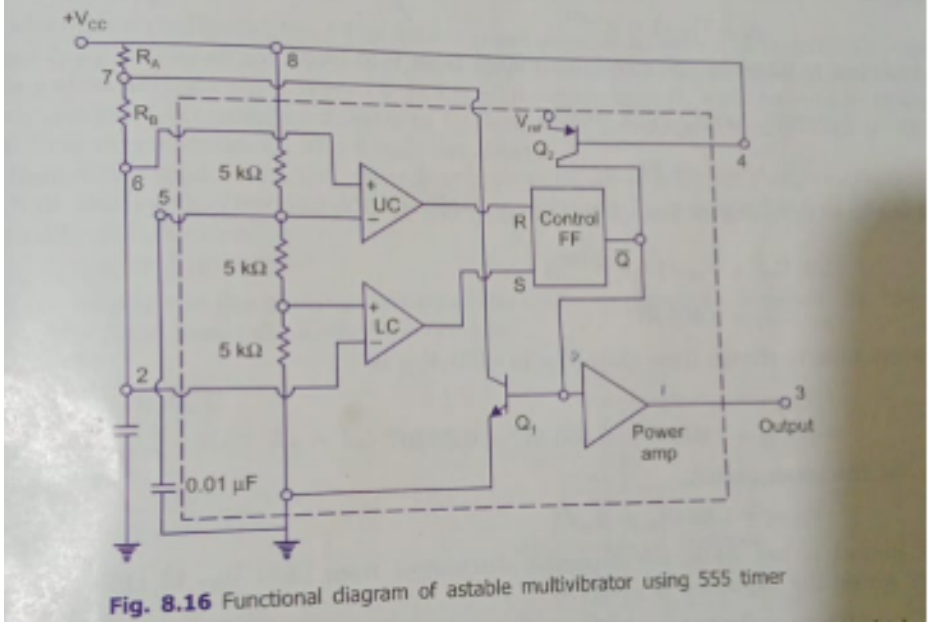
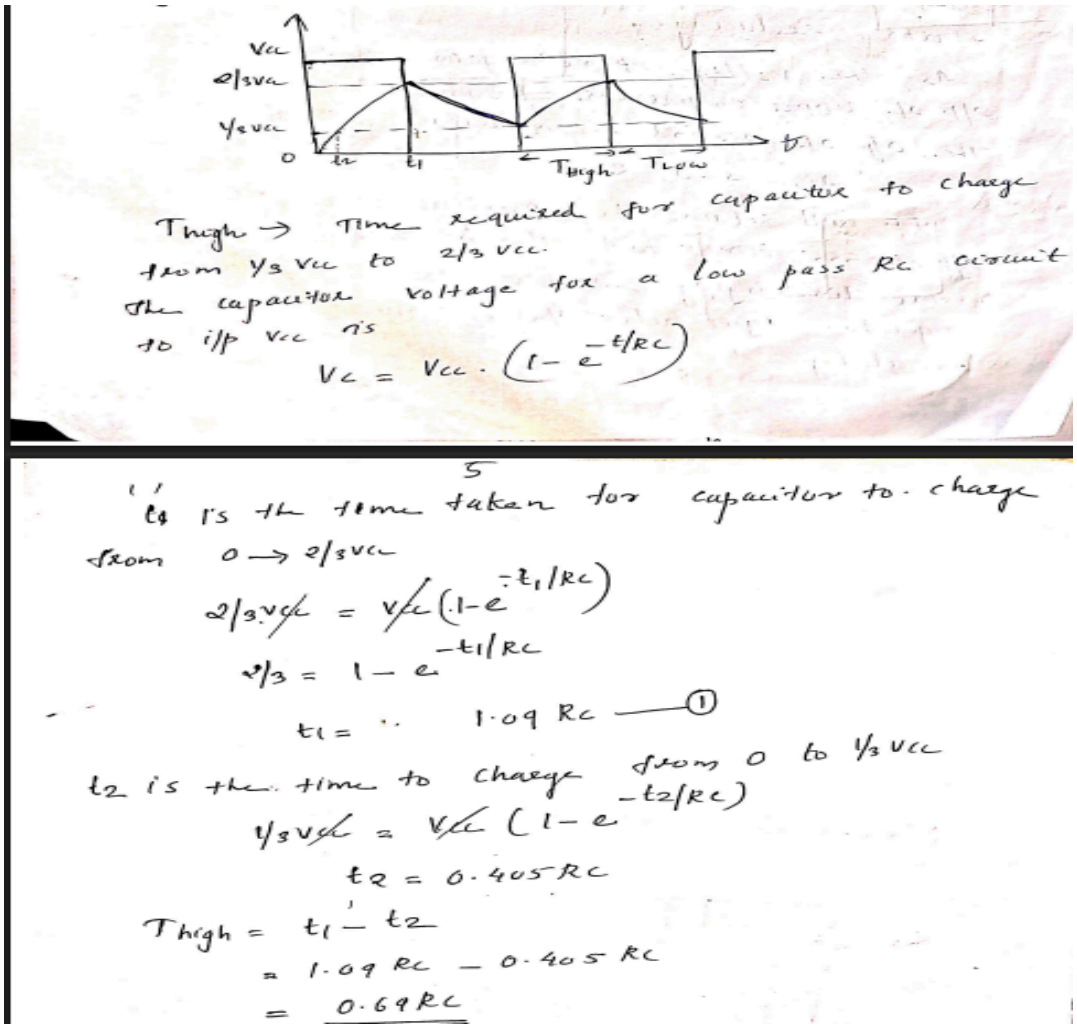


Fig. 8.16 Functional diagram of astable multivibrator using 555 timer

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free-running. However, the time during which the output is either high or low is determined by two resistors and a capacitor, which are externally connected to the 555 timer.

When the power supply Vcc is connected, the external timing capacitor C charges towards Vcc through R_A and R_B with time constant $(R_A+R_B)C$. During this time, output (pin 3) is high (equals Vcc) as Reset R=0, Set S=1 and this combination makes $\bar{Q}$ =0 which has unclamped the timing capacitor C.

When the capacitor voltage is just greater than 2/3 Vcc, the upper comparator triggers the control flip-flop so that R=1,S=0, $\bar{Q}$ =1 and Q=0. The output of astable is low. This, in turn, makes transistor Q1 on and capacitor starts discharging towards ground through R_B and transistor Q1 with a time constant R_BC. During the discharge of the timing capacitor , as it is just less than Vcc/3 , the lower comparator is triggered and at this stage S=1,R=0, which turns $\bar{Q}$ =0. The output of astable is high. Now $\bar{Q}$ =0 unclamps the external timing capacitor. The capacitor is thus periodically charged and discharged between and respectively. Then the cycle repeats



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b) Draw the pin diagram of 555 timer I.C. Design a monostable multivibrator using 555 timer I.C for a pulse width of 1 ms. Draw the circuit diagram. 7

3 marks for pin diagram +3 marks for design+1 mark for circuit diagram.

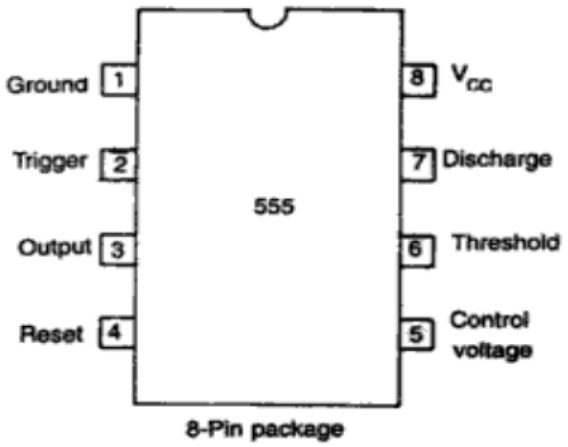

Fig. 8.1 Pin diagram

$T_p = 1.1\,RC$

Let C=0.1μF

R=8.2KΩ

$C_1 = 0.01\mu F$

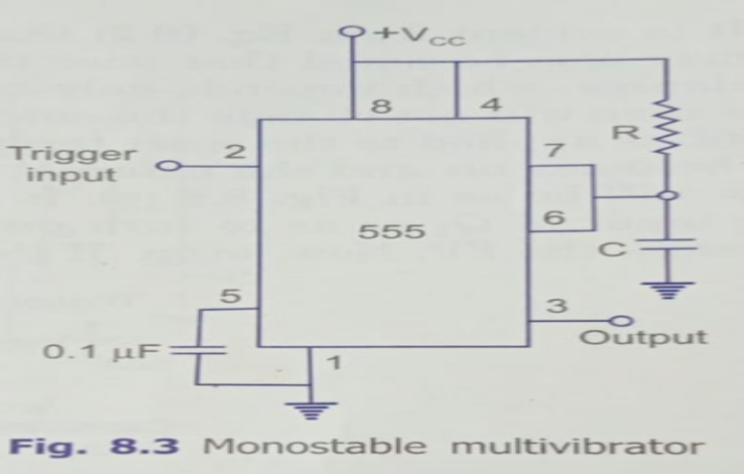

Fig. 8.3 Monostable multivibrator

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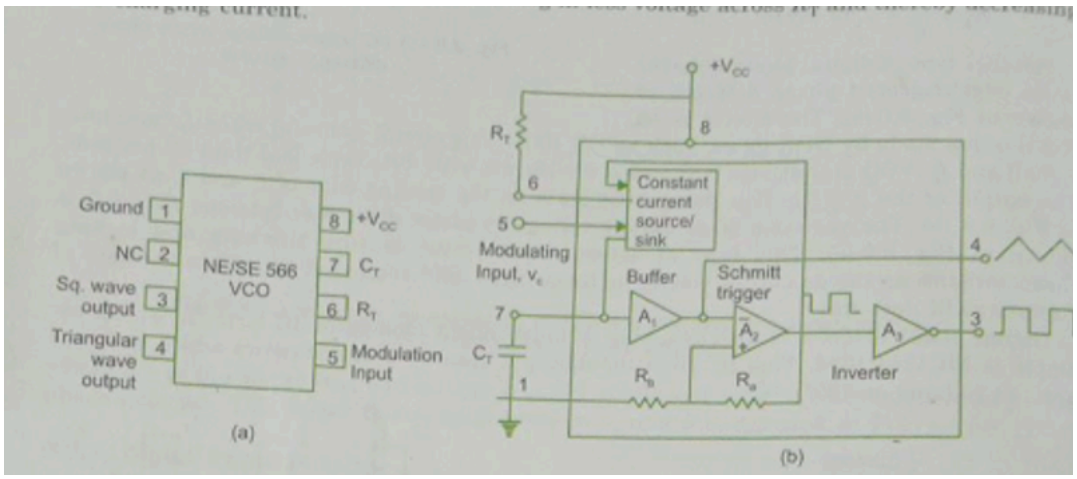
18 a) Explain the block diagram of Voltage Controlled Oscillator. Derive the equation for frequency of oscillation. 7

2 marks for block diagram+2 marks for working +3 marks for derivation



We know that, $q = CV$

$$i = \frac{dq}{dt}$$

$$i = \frac{d\,CV}{dt} = C \cdot \frac{dV}{dt}$$

$$\frac{i}{C_T} = \frac{dv}{dt} = \frac{\Delta V}{\Delta T}$$

$$\frac{i}{C_T} = \frac{0.5V_{cc} - 0.25V_{cc}}{\Delta T}$$

$$\frac{i}{C_T} = \frac{0.25V_{cc}}{\Delta T}$$

$$\Delta T = \frac{0.25 \cdot V_{cc} \cdot C_T}{i}$$

Total time period 'T' of the triangular waveforms $\Delta T + \Delta T = 2\Delta T$

$$f_0 = \frac{1}{2\Delta T} = \frac{1}{2}\left(\frac{i}{0.25 V_{cc} \cdot C_T}\right)$$

$$f_0 = \frac{i}{0.5 V_{cc} \cdot C_T}$$

$$i = \frac{V_{cc} - V_c}{R_T}$$

$$f_0 = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \quad \text{— (A)}$$

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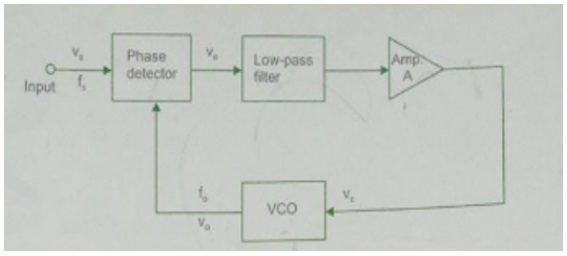
b) Using closed loop analysis, find the transfer function of the Phase Locked Loop. 7
3 marks for block diagram+ 4 marks for derivation



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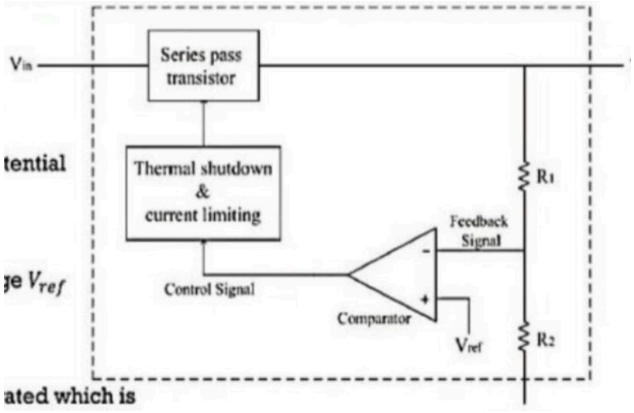
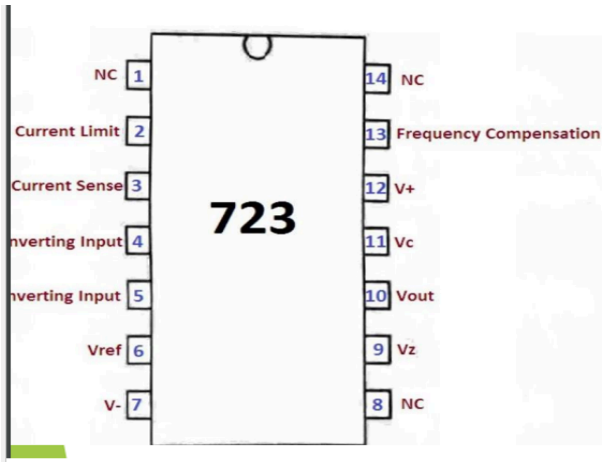
Module -5

19 a) Discuss the functional block diagram of 723 regulators. Draw the pin configuration of I.C 723. 7

3 marks for functional block diagram+ 2 marks for explanation+2 marks for pin configuration of I.C 723.





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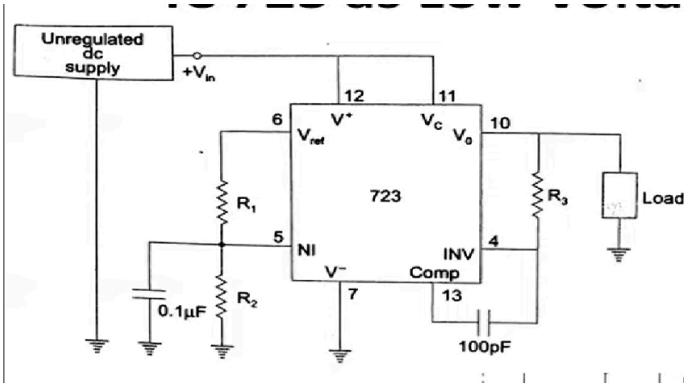
b) Using functional diagram, explain how regulation is achieved in low voltage regulators using 723. Draw the circuit diagram of low voltage regulator using 723 IC 7

2 marks for Functional diagram+3 marks for explanation+2 marks for circuit diagram.



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20 a) Explain the working of flash type ADC. 7

3 marks for diagram+4 marks for explanation

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b) An 8 bit Analog to Digital Converter accepts an input voltage signal of range 0 to 10V. What is the minimum value of the input voltage required to generate a change of 1 LSB.? Determine the input voltage required to generate all 1's at the output? 7

What is the digital output for an input voltage of 4.8 V

$1LSB = \frac{10V}{2^8}$=39.1mV (2 marks)

Maximum input voltage that can cause all 1's at the output=10V-39.1mV=9.961V (2 marks)

The digital output for an applied input voltage of 4.8 V is given by D = $\frac{4.8\,V}{39..1mV}$ = 123

Converting to binary, the digital output is 01111011 (3 marks)