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Total No. of Printed Pages: [01]

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B.Tech. (ECE) (Semester – 3rd)
DIGITAL ELECTRONIC CIRCUITS & DESIGN
Subject Code: BECES1-302
Paper ID: [18111311]

Time: 03 Hours

Maximum Marks: 60

Instruction for candidates:

1. Section A is compulsory. It consists of 10 parts of two marks each.
2. Section B consist of 5 questions of 5 marks each. The student has to attempt any 4 questions out of it.
3. Section C consist of 3 questions of 10 marks each. The student has to attempt any 2 questions.

Section – A

(2 marks each)

Q1. Attempt the following:

- a) Construct a truth table for the Boolean Expression $AC+BC$.
- b) Realize a NOR gate using NAND gates only.
- c) Describe the speed & power parameters of a TTL logic family.
- d) Demonstrate the utility of DeMorgan's Laws in digital logic circuit design.
- e) Construct a 4:1 Multiplexer using 2:1 Multiplexers.
- f) Compare and contrast analog and digital signal.
- g) Realize a 4-bit PISO based data transfer register.
- h) What is the difference between PAL and PLA?
- i) Illustrate a RS flip flop with preset and clear using NAND latch.
- j) Distinguish between Moore and Mealy model-based machines.

Section – B

(5 marks each)

- Q2. Find the output in Hexadecimal, if the three inputs given to an Exclusive NOR gate are 1A, 2B, and 3C respectively.
- Q3. What is a BCD code? Design a gate level 4-bit BCD adder combinational circuit.
- Q4. Describe various applications of Shift registers.
- Q5. Illustrate an edge triggered JK Flip Flop through Truth table, Excitation table, Characteristic equation and State Transition diagram.
- Q6. Explain the concept of state reduction and state assignment in finite state machines.

Section – C

(10 marks each)

- Q7. Simplify $Z = \sum m(0, 1, 3, 5, 6, 7, 10, 14, 15)$ and implement the simplified expression using NAND gates only.
- Q8. Design a full adder combinational circuit using (a) Multiplexers and (b) Decoders.

- Q9. Design a self-starting synchronous counter using D flip flops with counting sequence as 2, 6, 4, 0, 3 and repeat.