ECE 508: Verilog Workshop

Term Offered: Fall

Credits: 1

Course Description: This workshop will equip new graduate students with a basic understanding of SystemVerilog to help prepare them for the HDL-based graduate courses offered by the ECE department. Topics will include SystemVerilog syntax and simulation. Students will be given design and simulation assignments to complete.

Prerequisites: Graduate standing

Course Outcomes and Learning Goals
At the end of this workshop, students will be able to:

- Describe digital designs in the SystemVerilog HDL
- Successfully use logic simulation tools to debug and verify SystemVerilog-based hardware designs
- Refresh their understanding of digital system design

Please note that course content may change depending on the instructor of the workshop.