



SRI KRISHNA INSTITUTE OF TECHNOLOGY

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#57, Chimney Hills, Hesarahatta Main Road, Chikkabanavara Post, Bengaluru- 560090

Department of Electronics Engineering (VLSI D & T)

Academic Year	:	2026-27	Course Name	:	CAD for VLSI
Semester	:	7th	Course Code	:	BVL703
Scheme	:	2022	L: T: P: S	:	4:0:0:0 Credits:4
Total Contact hours	:	50 hrs	CIE Marks	:	50
Course Plan Author	:	Dr. N.C Patil	SEE Marks	:	50
Date	:	11.06.2026	Total Marks	:	100

Course Prerequisites:

- 1. Digital Electronics.
- 2. Synthesis basics and CAD tool knowledge
- 3. Digital VLSI design concepts

Course Objectives:

This course is designed to equip students with the following skills and knowledge:

- Apply graph theory to various phases of VLSI circuit physical design
- Understand and utilize graph-theoretic, heuristic, and genetic algorithms
- Explore and implement different optimization techniques
- Gain insight into key placement and routing methodologies

Course Outcomes:

CO	At the end of the course, students should be able to . . .		Blooms' Level
CO1	:	Demonstrate an understanding of various design methodologies in VLSI physical design	2
CO2	:	Apply graph-theoretic concepts to solve VLSI-related problems	2
CO3	:	Develop generalized algorithms for design automation	3
CO4	:	Implement the computational complexity of algorithms	3
CO5	:	Design and implement algorithms for VLSI automation tasks	3

Blooms' Taxonomy:

L1	L2	L3	L4	L5	L6
Remembering	Understanding	Applying	Analyzing	Evaluating	Creating



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Program Outcomes:

PO1	:	Engineering knowledge	PO7	:	Environment and sustainability
PO2	:	Problem analysis	PO8	:	Ethics
PO3	:	Design/development of solutions	PO9	:	Individual and team work
PO4	:	Conduct investigations of complex problems	PO10	:	Communication
PO5	:	Modern tool usage	PO11	:	Project management and finance
PO6	:	The engineer and society	PO12	:	Life-long learning

Program Specific Outcomes:

PSO1:	Graduates will possess advanced knowledge and practical skills in VLSI design including the use of state-of-the-art tools and techniques to develop, analyze and optimize analog, digital and mixed mode systems for real-world applications.
PSO2:	Graduates will demonstrate the ability to conduct interdisciplinary research in VLSI technologies contributing to innovative solutions that address global challenges while advancing sustainable and inclusive technology
PSO3:	Graduates will be equipped with the entrepreneurial mindset and leadership qualities necessary to create innovative solutions in VLSI design, promoting new ventures, generating employment and taking on roles that foster industry collaboration and societal impact.

CO-PO-PSO Mapping:

CO	Program Outcomes														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO12	PSO 1	PSO 2	PSO 3
CO1	3	2	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	2	3	3	-	2	-	-	-	-	-	-	-	3	-	-
CO3	3	3	2	2	2	-	-	-	-	-	-	-	2	-	-
CO4	3	2	3	2	3	-	-	-	-	-	-	-	2	-	-
CO5	3	2	3	2	3	-	-	-	-	-	-	-	2	-	-



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CO-PO Mapping justification

CO	PO / PSO	Correlation Weight age	Justification
CO1	PO1	3	CO1 requires students to apply fundamental engineering and subject-specific knowledge to understand the basic concepts and principles of the course.
	PO2	2	Students apply analytical and logical reasoning to understand and analyze problems related to the fundamental concepts covered in the course.
	PSO1	3	CO1 strongly contributes to the application of core Electronics/VLSI knowledge and fundamentals relevant to the program specialization.
CO2	PO1	2	Students apply engineering and domain knowledge to understand and analyze the concepts introduced in CO2.
	PO2	3	CO2 requires students to analyze technical problems systematically using appropriate principles, models, and methods.
	PO3	3	Students use engineering principles to develop and evaluate suitable solutions for problems related to the course concepts.
	PO5	2	Students use appropriate engineering tools, techniques, and computational/simulation methods to analyze the problems.
	PSO1	3	CO2 provides strong support for applying specialized Electronics/VLSI concepts in solving technical problems.
CO3	PO1	3	CO3 requires strong application of engineering and specialized domain knowledge for understanding and solving advanced course-related problems.
	PO2	3	Students analyze complex technical problems using appropriate engineering concepts and systematic procedures.
	PO3	2	Students apply design-oriented approaches to formulate suitable solutions based on the requirements and constraints of the problem.
	PO4	2	Students use appropriate analysis, experimentation, or simulation approaches to investigate and validate technical concepts.
	PO5	2	Students employ suitable modern engineering tools and techniques for analysis, design, simulation, or verification.
	PSO1	2	CO3 moderately contributes to the application of specialized knowledge and tools in Electronics/VLSI-related applications.



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CO4	PO1	3	CO4 requires strong application of engineering fundamentals and specialized knowledge to address course-related technical problems.
	PO2	2	Students analyze technical requirements and problems and use logical reasoning to arrive at appropriate solutions.
	PO3	3	CO4 strongly supports the development, evaluation, and selection of appropriate engineering solutions considering relevant requirements and constraints.
	PO4	2	Students investigate technical problems through analysis, experimentation, simulation, or interpretation of results.
	PO5	3	CO4 strongly involves the selection and effective use of modern engineering tools, software, simulation techniques, or computational methods.
	PSO1	2	CO4 contributes to applying specialized Electronics/VLSI knowledge and techniques to practical engineering problems.
CO5	PO1	3	CO5 requires strong application of engineering fundamentals and specialized subject knowledge to solve advanced technical problems.
	PO2	2	Students analyze technical problems and evaluate alternative approaches using appropriate engineering principles.
	PO3	3	Students develop and evaluate appropriate engineering solutions by considering technical requirements and practical constraints.
	PO4	2	Students investigate and validate solutions using analytical, experimental, or simulation-based approaches.
	PO5	3	CO5 requires effective application of modern engineering tools, simulation software, computational techniques, or other appropriate technologies.
	PSO1	2	CO5 contributes to the application of specialized Electronics/VLSI knowledge and techniques in solving practical engineering problems.



Course Content (Syllabus)

Module 1	CH
Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies. [Text1: 1.1,1.2,1.3,1.4] VLSI Design Automation tools: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools.[Text1: 2.1,2.2,2.3,2.4,2.5,2.6]	10
Module 2	
Algorithmic graph theory and computational complexity: Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. [Text1: 3.1,3.2,3.3,3.4] Tractable and intractable problems: Combinational optimization problems, Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences. [Text1: 3.1,3.2,3.3,3.4,3.5].	10
Module 3	
Partitioning: Problem formulation, Classification of Partitioning Algorithms. [Text2: 4.1, 4.2] Group migration algorithms: Kernighan-Lin algorithm, Simulated Annealing, Simulated Evolution. [Text2: 4.3,4.31, 4.4,4.41,4.42] Placement: Problem formulation, Classification of Placement Algorithm. [Text2: 5.1, 5.1.1, 5.1.2] Floor Planning: Problem formulation, Classification of Floor planning Algorithms, Constraint based floor planning, Rectangular dualization. [Text2: 5.2, 5.2.1, 5.2.2, 5.2.3]	10
Module 4	
Global Routing: Problem formulation, Classification of Global routing algorithms, Maze routing algorithms:Lee's algorithm, Soukup's algorithm and Hadlock's Algorithm, Line probe algorithms. [Text2: 6.1, 6.2, 6.3, 6.4] Detailed Routing: Problem formulation, Routing considerations, models, channel routing and switch box routing problems, Single-Layer Routing Algorithms, General river routing problem, Single row routing problem, Two-layer channel routing algorithms: Basic Left Edge Algorithm, Dogleg router, Symbolic router-YACR2. [Text2: 7.1, 7.3.1, 7.3.2, 7.4,7.4.2.1, 7.4.2.2]	10
Module 5	
Simulation and Logic Synthesis: Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis. [Text1:10.1,10.2, 10.3, 11.1, 11.2, 11.3]	10



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Schedule of Instruction:

Class No	Topic	Date	RBT	CO	Mode
Module-1					
Chapter Name					
1.	Introduction of course website: OBE knowledge	21.07.26			PPT
2.	Introduction of subject: Importance & MOOC's	22.07.26			PPT
3.	Introduction to Design Methodologies: The VLSI Design Problem,	23.07.26	L2	CO1	L
4.	The Design Domains,	24.07.26	L2	CO1	L
5.	Design Actions,	28.07.26	L2	CO1	V+L
6.	Design Methods and Technologies.	29.07.26	L2	CO1	L
7.	VLSI Design Automation tools:	30.07.26	L2	CO1	L
8.	Algorithmic and System Design, Structural and Logic Design	31.07.26	L3	CO1	PPT
9.	Transistor-level Design	04.08.26	L2	CO1	L
10.	Layout Design	05.08.26	L3	CO1	L
11	Verification Methods, Design	06.08.26	L2	CO1	L
12	Management Tools	07.08.26	L3	CO1	L
Module-2					
Chapter Name					
13	Algorithmic graph theory and computational complexity: Terminology,	11.08.26	L2	CO2	L
14	Data Structures for the Representation of Graphs	12.08.26	L2	CO2	L
15	Computational Complexity,	13.08.26	L2	CO2	L
16	Examples of Graph Algorithms	14.08.26	L2	CO2	L
17	Tractable and intractable problems:	18.08.26	L3	CO2	L
18	Combinational optimization problems	19.08.26	L3	CO2	L
19	Decision Problems,	20.08.26	L2	CO2	L
20	Complexity Classes,	25.08.26	L2	CO2	L
21.	NP-completeness and NP-hardness	27.08.26	L2	CO2	L
22	Consequences	28.08.26	L2	CO2	L
Module-3					
Chapter Name					
23	Group migration algorithms: Kernighan-Lin algorithm,	01.09.26	L2	CO3	
24	Simulated Annealing, Simulated Evolution.	02.09.26	L2	CO3	L
25	Partitioning: Problem formulation,	03.09.26	L2	CO3	L
26	Classification of Partitioning Algorithms.	04.09.26	L3	CO3	L
27	Placement: Problem formulation,	08.09.26	L3	CO3	L
28	Classification of Placement Algorithm	09.09.26	L3	CO3	L
29	Floor Planning: Problem formulation,	16.09.26	L2	CO3	L
30	Classification of Floor planning Algorithms,	17.09.266	L2	CO3	L
31	Rectangular dualization.	18.09.26	L2	CO3	L
32	Rectangular dualization.	22.09.26			
Module-4					
Chapter Name					



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Class No	Topic	Date	RBT	CO	Mode
33	Global Routing: Problem formulation, Classification of Global routing algorithms	23.09.26	L2	CO4	PPT
34	Maze routing algorithms:	24.09.26	L3	CO4	L
35	Logic Synthesis for Low Power estimation techniques:	25.09.26	L2	CO4	L
36	Line probe algorithms	29.09.26	L3	CO4	L
37	Detailed Routing: Problem formulation, Routing considerations,	30.09.26	L3	CO4	L
38	models, channel routing and switch box routing problems,	01.10.26	L2	CO4	L
39	Single-Layer Routing Algorithms,	06.10.26	L2	CO4	L
40	General river routing problem, Single row routing problem,	07.10.26	L2	CO4	L
41	Two-layer channel routing algorithms: Basic Left Edge Algorithm,	08.10.26	L2	CO4	L
42	Dogleg router, Symbolic router-YACR2.	09.10.26	L2	CO4	L
Module-5					
Chapter Name					
43	Simulation and Logic Synthesis:Simulation	06.10.26	L2	CO5	PPT
44	Gate-level modeling and simulation,	07.10.26	L3	CO5	L
45	Gate-level modeling and simulation,	08.10.26	L3	CO5	L
46	Switch-level modeling and simulation,	09.10.26	L2	CO5	L
47	Switch-level modeling and simulation,	13.10.26	L3	CO5	L
48	Combinational Logic Synthesis	14.10.26	L2	CO5	L
49	Combinational Logic Synthesis	15.10.26	L2	CO5	L
50	Binary Decision Diagrams,	16.10.26	L3	CO5	L
51	Binary Decision Diagrams,	22.10.26	L2	CO5	L
52	Two Level Logic Synthesis	23.10.26	L3	CO5	L

Self-study hours:

For 4 credits: Self-study hours = 120 hours – Course delivery planned hours = ... hours

For 3 credits: Self-study hours = 90 hours – Course delivery planned hours = ... hours

For 2 credits: Self-study hours = 60 hours – Course delivery planned hours = ... hours

For 1 credit: Self-study hours = 30 hours – Course delivery planned hours = ... hours

SL#	Self-study content	Hours
1	NPTEL/ Udemy Course/Maven Silicon	30 Hrs
2	Assignment	20Hrs
3	CAD Tools Learning-Implementation with Synopsys tools	20Hrs
Total hours		70Hrs



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Textbooks:

T1	S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2nd Edition.
T2	N. Sherwani, Algorithms for VLSI Physical Design Automation, KAP, 1999.
T3	Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, "Handbook of Algorithms for Physical Design Automation, CRC Press, 1st Edition, 2.

Reference books:

R1	
R2	

Web links and Video Lectures (e-Resources):

1.	https://tinyurl.com/yc6x5myf (Course Website)
2.	Notes by KiaBazargan from Univ. of Minnesota [©Bazargan] • http://www.ece.umn.edu/users/kia/Courses/EE5301
3.	– Notes by Kurt Keutzer from UC-Berkeley [©Keutzer] • http://www-cad.eecs.berkeley.edu/~niraj/ee244/index.htm – Notes by Rajesh Gupta, UC-San Diego [©Gupta] • http://www.ics.uci.edu/~rgupta/ics280.html

Assessment Schedule:

S.N	Assessment Type	Content	CO	Duration	Marks	Date
11.	IA Test 1	Module 1, 2 & 3(Part I)	1,2,3	1.30 min	50	11.09.26
12.	IA Test 2	Module 3(Part II) 4 & 5	3,4,5	1.30 min		27.10.26
IA Scaled down to					25	
IA Theory component						
13.	Unit Test	Module 1, 2	1,2	1 hour	10	23.09.26
14.	Unit Test	Module 4,5	3,4	1 hour	10	20.10.26



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23	Quiz	Module 1,2,3,4,5	1,2,3,4	20Min	05	21.10.26
Assessment Total					25	
Total (IA + Assessment)					50	
15.	Semester End Examination				100	
SEE Scaled down to					50	
Total (IA+ SEE)					100	

RB – Text Book/Reference Book, **L* – Interactive Lecture, *V*- Videos or any other mode, **RBT* – Revised Blooms' Taxonomy, *L: T: P:*
C – Theory/Lecture: Tutorial: Practical/Drawing: Credits, *SEE*: Semester End Examination, *CIE*: Continuous Internal Evaluation

****Kindly mention Assessment Structure based on the course***

Faculty In charge

Course Coordinator

HoD