BANGALORE INSTITUTE OF TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
LESSON PLAN

SUB: Advanced Computer Architectures	**SUB CODE: 17CS72**
SEM: 7 'B'	**IA MARKS: 40**
TOTAL NO. OF LECTURE HOURS: 50	**MAX MARKS: 40**
PRE REQUISITES	
1. Computer Organization (17CS34).	**2. Microprocessors and Microcontrollers(17CS44)**

Hour	Topic to be covered	Levels
	MODULE I	
1	CHAPTER I: Parallel Computer Models-: Review of computer organization, microprocessor and microcontrollers, Importance of Computer Architecture in life.	L1
2	State of Computing, evolution of computer architecture- Flynn's classification	L2
3	System and Performance Attributes, Classification of multi computers and multiprocessors	L2
4	SIMD Computers, PRAM and VLSI Models	L2
5	Program and Network Properties -Conditions of Parallelism	L2
6	Program Partitioning and Scheduling, Program Flow Mechanisms	L2
7	System Interconnect Architectures	L2
8	Principles of Scalable Performance, Performance Metrics and Measures	L2
9	Parallel Processing Applications, Speedup Performance Laws	L2
10	Scalability Analysis and Approaches.	L2
	MODULE II	
11	Hardware Technologies: Processors and Memory Hierarchy	L1, L2
12	Advanced Processor Technology, Superscalar Processors	L2
13	Vector processors, Memory Hierarchy Technology	L2
14	Virtual Memory Technology, page replacement algorithms-LRU, OPT, FIFO	L2, L3
	MODULE III	
15	Introduction to bus, Cache, and Shared Memory	L1, L2
16	Organization of bus systems, cache memory and shared memory with an example each	L2
17	Sequential and Weak Consistency Models	L2
18	Pipelining and Superscalar Techniques	L2
19	Linear Pipeline Processors, Nonlinear Pipeline Processors	L2, L3
20	Design of a instruction Pipeline, Arithmetic Pipeline with an example	L2, L3
	MODULE IV	
21	Introduction to Multiprocessor System Interconnects	L1
22	Cache Coherence and Synchronization Mechanisms	L2
23	Three Generations of Multicomputer and Message-Passing Mechanisms	L2
24	Vector Processing Principles along with SIMD	L2
25	Multivector Multiprocessors, Compound Vector Processing	L2
26	SIMD Computer Organizations, Scalable systems	L2
27	Multithreaded, and Dataflow Architectures	L2
28	Latency-Hiding Techniques, Principles of Multithreading	L2

29	Fine-Grain Multicomputers, Scalable and Multithreaded Architectures	L2
30	Hybrid architectures with an example	L2
	MODULE V	
31	Introduction to Software for parallel programming: Parallel Models	L1
32	Explanation of different languages and compilers available	L2
33	Parallel programming models-architectures with an example	L2
34	Detailed explanation of parallel languages and compilers	L2
35	Dependence Analysis of Data Arrays, environments	L2
36	Instruction and System Level Parallelism, Instruction Level Parallelism	L2
37	Operand Forwarding, Reorder Buffer	L2, L3
38	Register Renaming, tomasulo's algorithm	L2, L3
39	Branch Prediction details	L2
40	Synchronization and Multiprocessing Modes	L2
41	Instruction level Parallelism- computer architecture	L2
42	Basic Design issues	L2
43	Problem Definition	L2
44	Model of a typical processor	L2
45	Compiler Detected Instruction level parallelism	L2
46	Operand forwarding	L2
47	Recorder Buffer	L2
48	Register Renaming, Tomosulo's algorithm for branch prediction	L2, L3
49	Limitations in Exploiting Instruction Level Parallelism	L2
50	Thread Level Parallelism details and discussion of previous Question papers	L2

Faculty In-charge

Course Coordinator