DIODE CLAMP MULTILEVEL INVERTER

EXPERIMENT NO: **DATE:**

AIM : STUDY THE OPERATION AND PERFORMANCE OF 3-LEVEL DIODE CLAMP MULTILEVEL INVERTER USING LEVEL SHIFTED MULTI CARRIER MODULATION IN MATLAB.

THEORY:

Fig.1 3-level diode clamped MLI (one-phase only)

S1	S2	S1'	S2'	Vao
1	1	0	0	
0	1	1	0	
0	0	1	1	
0	0	1	1	
0	0	1	1	

Table1-1: Switching states of 3- level inverter

Voltage level	Active switches	Clamping diodes	Dc Capacitors
m	6(m-1)	3(m-1)(m-2)	(m-1)
5	24	36	4

Table-2: Component count for 5-level inverters

Simulink Model of 5- Level Diode Clamped Inverter

Specification:

Vdc Volatege: 300V

Carrier Frequency: 2Khz

DC Link Capacitor C1 – C4 = $1200e^{-6}$

Fig. 2 Simulink Model for 3-Level Diode Clamp Inverter for R-Phase

Fig. 2 Carrier & Reference Signals for S1 & S2 Switches and gate pulses

Simulation Results:

Fig. 3(a) Phase Voltage for R/Y/B Phase

Fig. 3(b) Line Voltages of V_{RY}/ V_{BY} /V_{RB}

Fig. 3(c) Phase current for R-Phase

Fig. 3(d) FFT spectra for phase voltages and current

Observation table:

1) R Load

Modulating wave (peak)	V_{ph} (peak)	V_{ph} THD(%)	V_{ll} (Peak)	V_{ll} THD(%)	I_{ph} (peak)	I_{ph} THD (%)

2) R-L Load

Modulating wave (peak)	V_{ph} (peak)	V_{ph} THD(%)	V_{ll} (Peak)	V_{ll} THD(%)	I_{ph} (peak)	I_{ph} THD (%)

CONCLUSION:

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SIGN: **MARKS:**

CHB MULTILEVEL INVERTER (LEVEL SHIFT)

EXPERIMENT NO: **DATE:**

AIM: TO STUDY AND SIMULATE CASCADED HALF BRIDGE FIVE LEVEL INVERTER USING LEVEL SHIFTING MULTICARRIER MODULATION.

THEORY:

As the name suggests, the cascaded H-bridge multilevel inverter uses multiple units of H-bridge power cells connected in a series chain to produce high ac voltages. A typical configuration of a five-level CHB inverter is shown in Fig.1, where each phase leg consists of two H-bridge cells powered by two isolated dc supplies of equal voltage E. The dc supplies are normally obtained by multiples diode rectifiers.

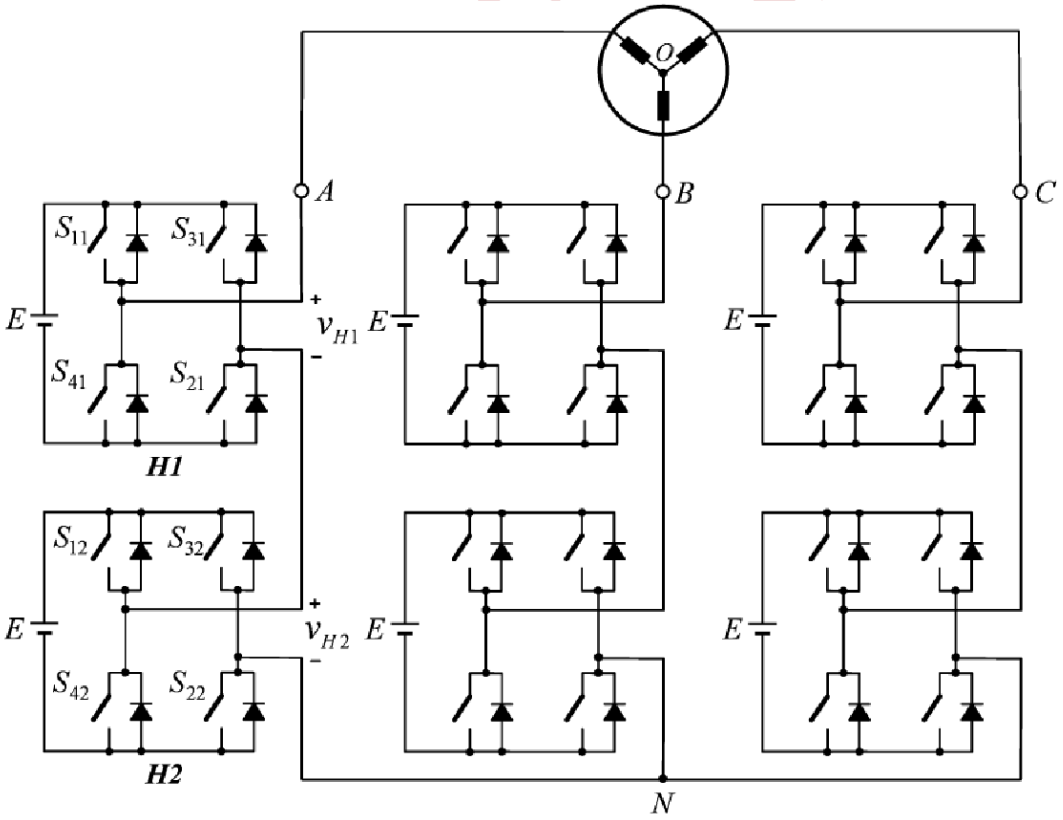


Figure.1: Five-level cascaded H-bridge inverter.

The cascaded half bridge inverter in figure can produce a phase voltage with five voltage levels. When switches S11,S21,S12, and S22 conduct, the output voltage of the half bridge cells H1 and H2 is $V_{H1} = V_{H2} = E$, and the resultant inverter phase voltage is $V_{AN} = V_{H1} + V_{H2} = 2E$, which is the voltage at the inverter terminal A with respect to the inverter neutral N.

Similarly, with S31, S41, S32, and S42 switched on, $V_{AN} = -2E$.
V_{AN} may not necessarily equal the load phase voltage V_{AO}, which is the voltage at node A with respect to the load neutral O.

The number of voltage levels in a cascaded half bridge inverter can be found from,

$$m = (2H + 1)$$

where, H is the number of H-bridge cells per phase leg. The voltage level m is always an odd number for the cascaded half bridge inverter while in other multilevel topologies such as diode-clamped inverters, it can be either an even or odd number.

The cascaded half bridge inverter introduced above can be extended to any number of voltage levels. The per-phase diagram of seven- and nine-level inverters are depicted in Fig.2(a), where the seven-level inverter has three H-bridge cells in cascade while the nine-level has four cells in series.

The total number of active switches (IGBTs) used in the cascaded half bridge inverters can be calculated by

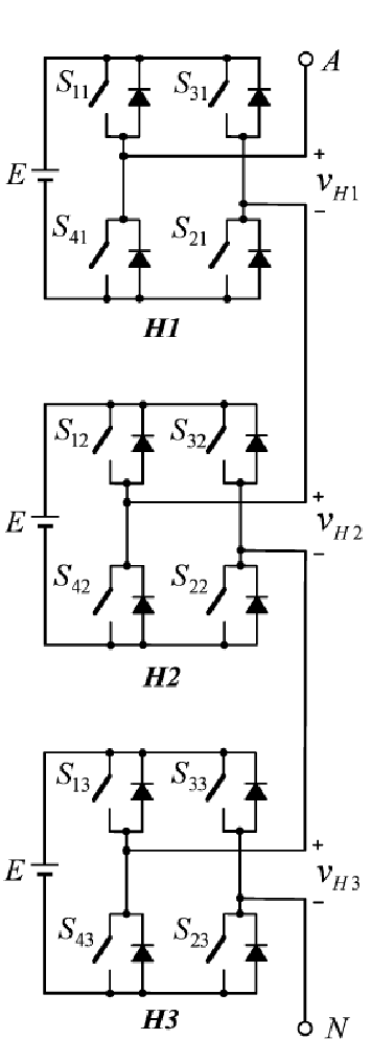
$$Nsw = 6(m - 1)$$

CARRIER-BASED PWM SCHEMES

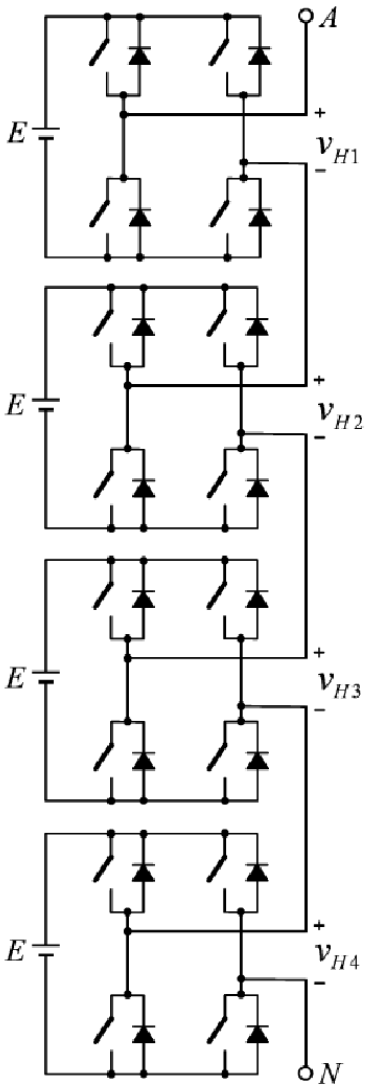
The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the CHB inverters.

Level-Shifted Multicarrier Modulation

Similar to the phase-shifted modulation, an m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m – 1) triangular carriers, all having the same frequency and amplitude. The (m – 1) triangular carriers are vertically disposed such that the bands they occupy are contiguous.



(a) Seven-level inverter



(b) Nine-level inverter

Figure.2: Casceded Multilevel Inverter for 7 Level & 9 Level Configuration

Figure2. shows the principle of the IPD modulation for a seven-level CHBinverter operating under the condition of mf = 15, ma = 0.8, fm= 60 Hz, and fcr= fm× mf = 900 Hz. The uppermost and lowermost carrier pair, vcr1 and vcr1–, are used to generate the gatings for switches S11 and S31 in power cell H1 of Fig. a. The innermost carrier pair, vcr3 and vcr3–, generate gatings for S13 and S33 in H3. The remaining carrier pair, vcr2 and vcr2–, are for S12 and S32 in H2. For the carriers above the zero reference (vcr1, vcr2, and vcr3), the switches S11, S12, and S13 are turned on when the phase A modulating signal vmAis higher than the corresponding carriers.

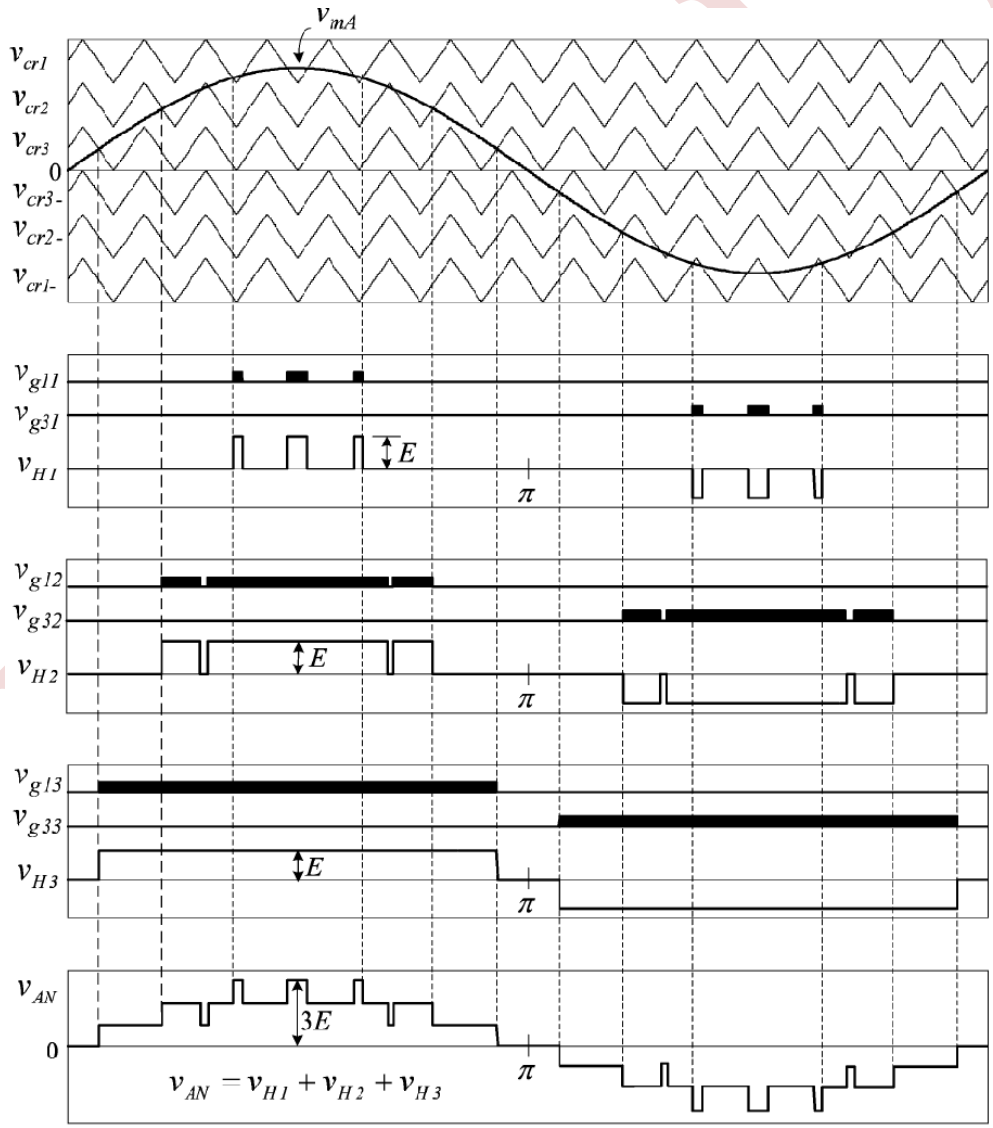


Figure.3: Level shifted PWM for seven level CHB inverter

For the carriers below the zero reference (vcr1–, vcr2–, and vcr3–), S31, S32, and S33 are switched on when V_{mA} is lower than the carrier waves. The gate signals for the lower switches in each H-bridge are complementary to their corresponding upper switches, and thus for simplicity they are not shown. The resultant H-bridge output voltage waveforms V_{H1}, V_{H2}, and V_{H3} are all unipolar as shown in Fig. 3. The inverter phase voltage waveform V_{AN} is formed with seven voltage levels.

Fig. 4 Simulink Model for Cascaded 5 Level Inverter

Figure. 5 Carrier & Reference Signals for Cascaded 5 Level Inverter

Figure 6(a). Output Phase Voltage

Figure 6(b). Output Line Voltage

Figure 6(c). Phase Current

Figure 6(d). FFT Spectrum (Phase voltages & Line current)

Observation table:

1)

fc=_____

Modulating wave (peak)	V_{ph} (peak)	V_{ph} THD(%)	V_{ll} (Peak)	V_{ll} THD(%)	I_{ph} (peak)	I_{ph} THD (%)

CONCLUSION:

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SIGN: **MARKS:**

CHB MULTILEVEL INVERTER (PHASE SHIFT)

EXPERIMENT NO: **DATE:**

AIM: TO STUDY AND SIMULATE CASCADED HALF BRIDGE FIVE LEVEL INVERTER USING PHASE SHIFTING MULTICARRIER MODULATION.

THEORY:

PHASE-SHIFTED MULTICARRIER MODULATION FOR 5 LEVEL CHB MLI

In general, a multilevel inverter with m voltage levels requires (m – 1) triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by:

$$\phi_{cr} = \frac{360^o}{(n-1)}$$

Figure 2 shows the principle of the phase-shifted modulation for a seven level CHB inverter, where six triangular carriers are required with a 60° phase displacement between any two adjacent carriers. Of the three-phase sinusoidal modulating waves, only the phase A modulating wave Vma is plotted for simplicity. The carriers vcr1, vcr2, and vcr3 are used to generate gatings for the upper switches S11, S12, and S13 in the left legs of power cells H1, H2, and H3 in Fig. 7.3-2a, respectively. The other three carriers, vcr1–, vcr2– and vcr3–, which are 180° out of phase withvcr1, vcr2 and vcr3, respectively, produce the gating for the upper switches S31, S32,and S33 in the right legs of the H-bridge cells. The gate signals for all the lower switches in the H-bridge legs are not shown since these switches operate in a complementary manner with respect to their corresponding upper switches.

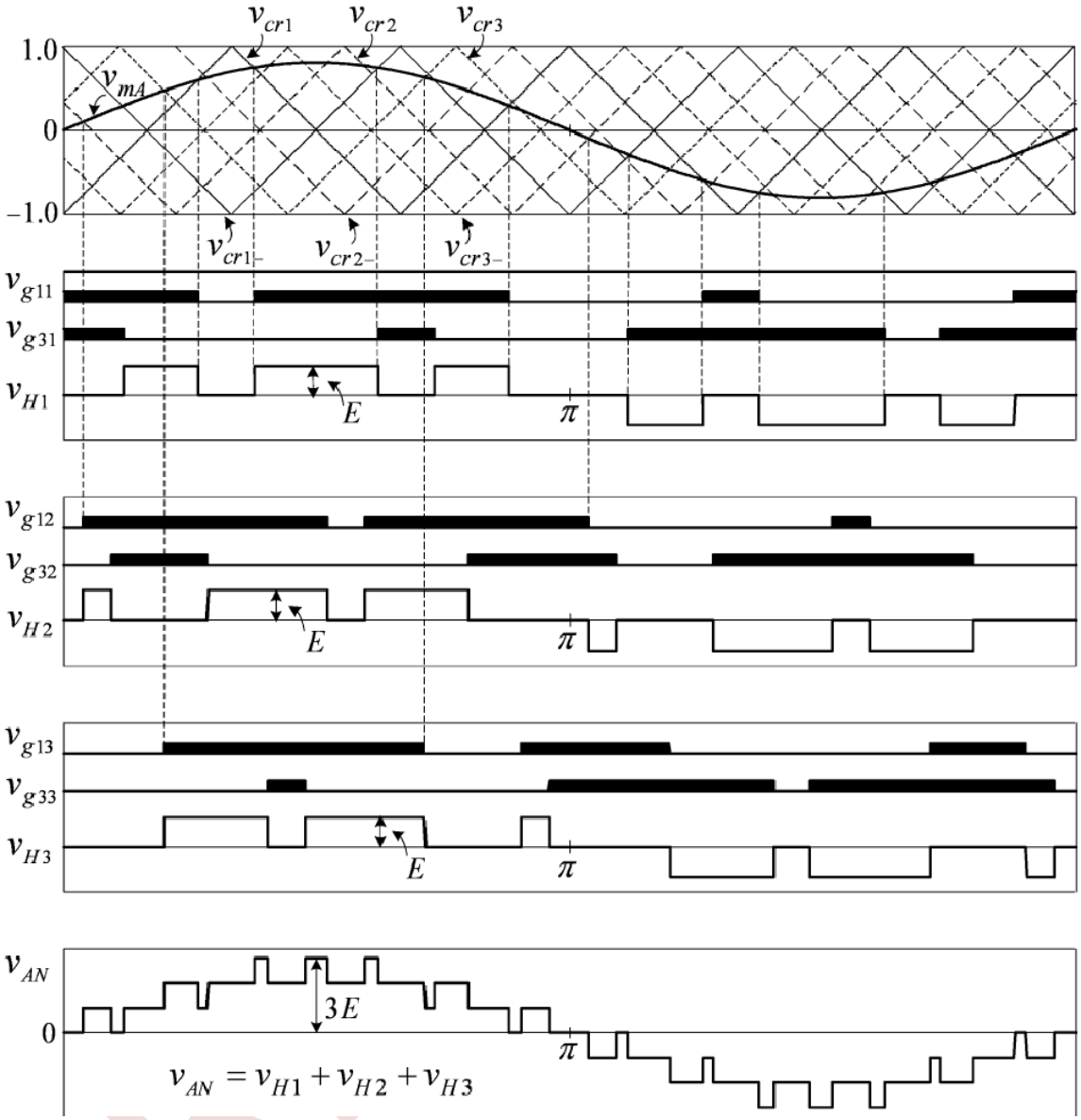

Figure:2 Phase-shifted PWM for seven-level CHB inverters (mf = 3, ma = 0.8, fm = 60 Hz, and fcr = 180 Hz).

The inverter phase voltage can be found from

VAN = vH1 + vH2 + vH3

Where vH1, vH2, and vH3 are the output voltages of cells H1, H2, and H3, respectively.

It is clear that the inverter phase voltage waveform is formed by seven voltage steps: +3E, 2E, E, 0, –E, –2E, and –3E.

Fig. 3 Simulink Model for Cascaded 5 Level Inverter

Figure. 4 Carrier & Reference Signals for Cascaded 5 Level Inverter

Figure 5(a). Output Phase Voltage

Figure 5(b). Output Line Voltage

Figure 5(c). Phase Current

Figure 5(d). FFT Spectrum (Phase Voltage & Current)

Observation table:

1)

fc=_____

Modulating wave (peak)	V_{ph} (peak)	V_{ph} THD(%)	V_{ll} (Peak)	V_{ll} THD(%)	I_{ph} (peak)	I_{ph} THD (%)

Results and discussion:

THE FOLLOWING TEXT SHOULD BE HANDWRITTEN:

>The H-bridge output voltages, *vH*1, *vH*2, and *vH*3, produced by the phase-shifted modulation are almost identical except a small phase displacement among them. All the devices operate at the same switching frequency and conduction time.

Table 7.4-1 Comparison Between the Phase- and Level-Shifted PWM Schemes

Comparison	Phase-Shifted Modulation	Level-Shifted Modulation (IPD)
Device switching frequency	Same for all devices	Different
Device conduction period	Same for all devices	Different
Rotating of switching patterns	No required	Required
Line-to-line voltage THD	Good	Better

CONCLUSION:

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SIGN: **MARKS:**

BUCK CONVERTER

EXPERIMENT NO: **DATE:**

AIM: TO STUDY AND SIMULATE BUCK CONVERTER.

THEORY:

Fig. 1 Simulink Model of buck converter

Fig. 2 Simulation results of buck converter

Observation table:

Buck Converter

Input Voltage=_____

Switching frequency=_____

Sr No	duty ratio	Output Votage (Simulation)	Output Votage (Calculated)

CONCLUSION:

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SIGN: **MARKS:**

BOOST CONVERTER

EXPERIMENT NO: **DATE:**

AIM: TO STUDY AND SIMULATE BOOST CONVERTER.

THEORY:

Fig. 1 Simulink Model of boost converter

Fig. 2 Simulation results of boost converter

Observation table:

Boost Converter

Input Voltage=_____

Switching frequency=_____

Sr No	duty ratio	Output Votage (Simulation)	Output Votage (Calculated)

CONCLUSION:

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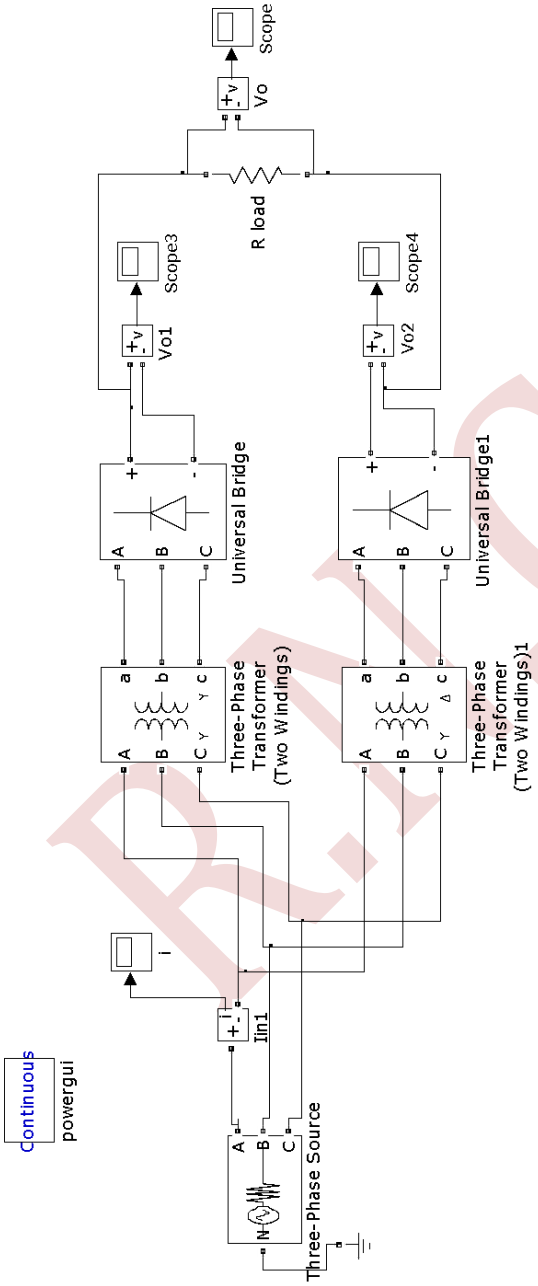
SIGN: **MARKS:**

3 ø MULTIPULSE CONVERTER

EXPERIMENT NO: **DATE:**

AIM: TO SIMULATE 3 ø MULTIPULSE CONVERTER USING MATLAB

SIMULINK MODEL:



RESULTS:

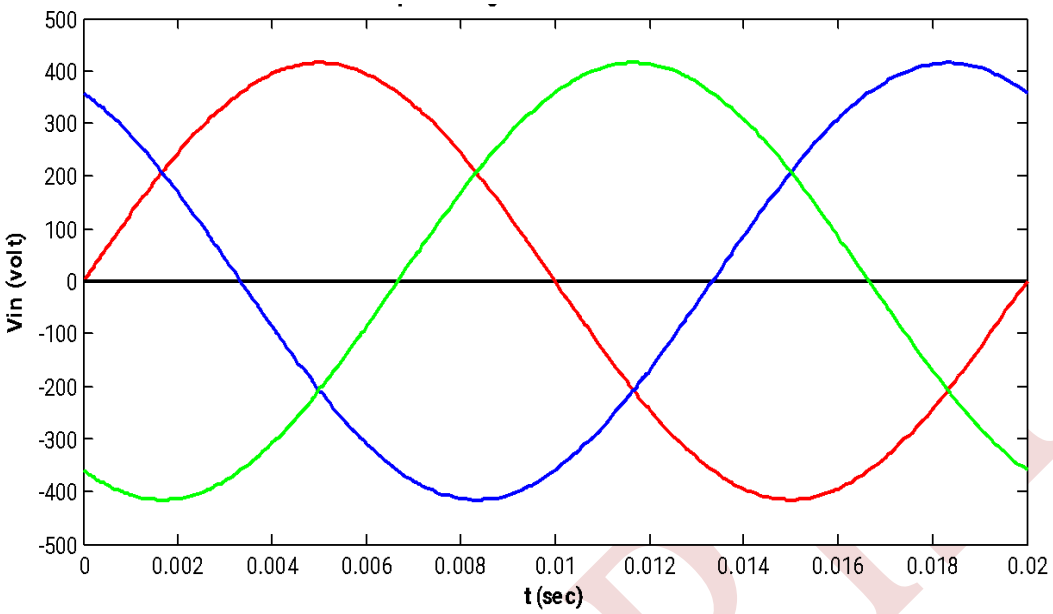


Fig (a) Input voltage

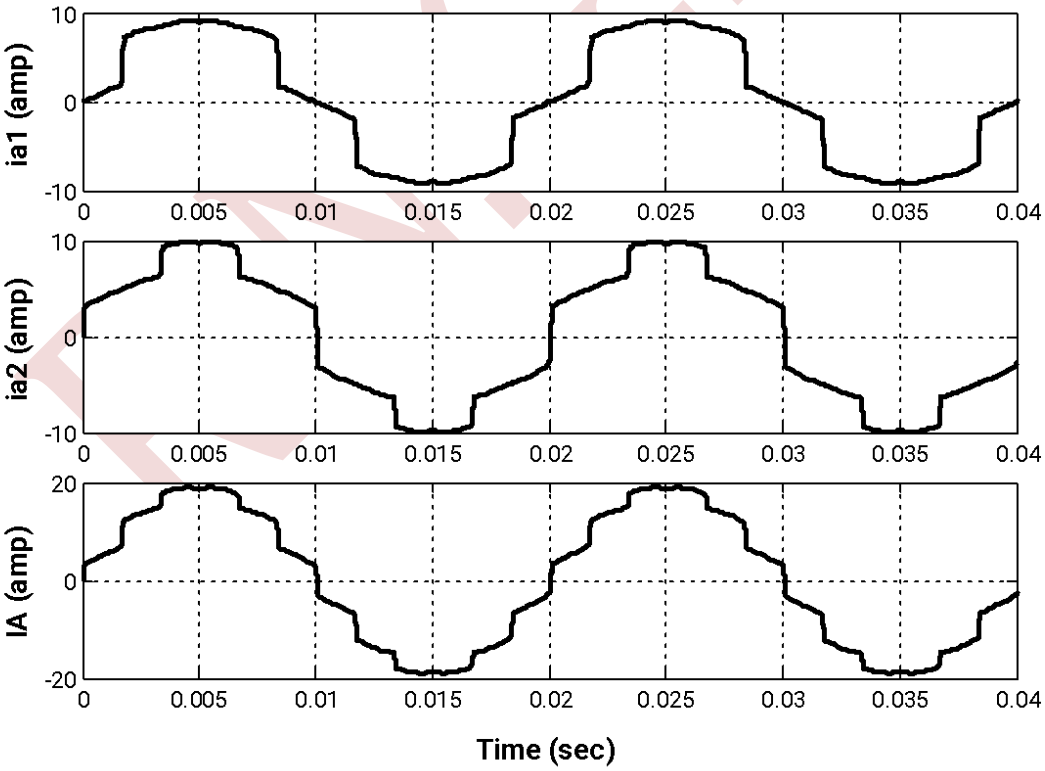


Fig (b) Input current

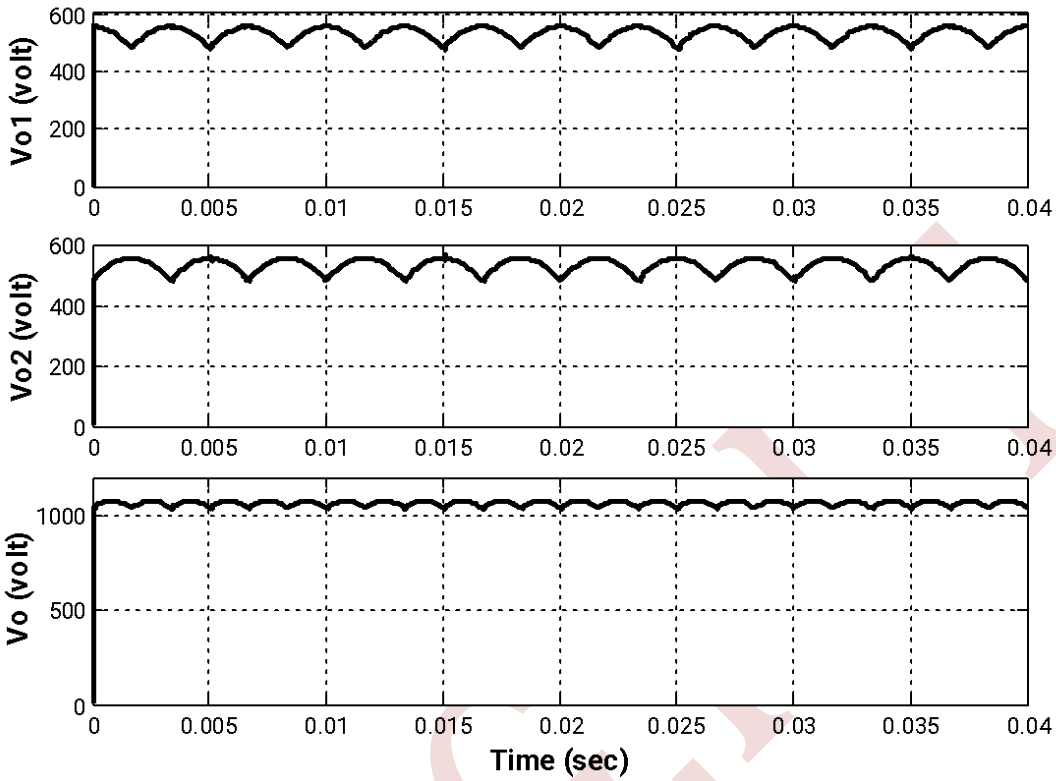


Fig (c) Output voltage

CONCLUSION:

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SIGN: **MARKS:**

MULTILEVEL INVERTER IN SQUARE WAVE MODE

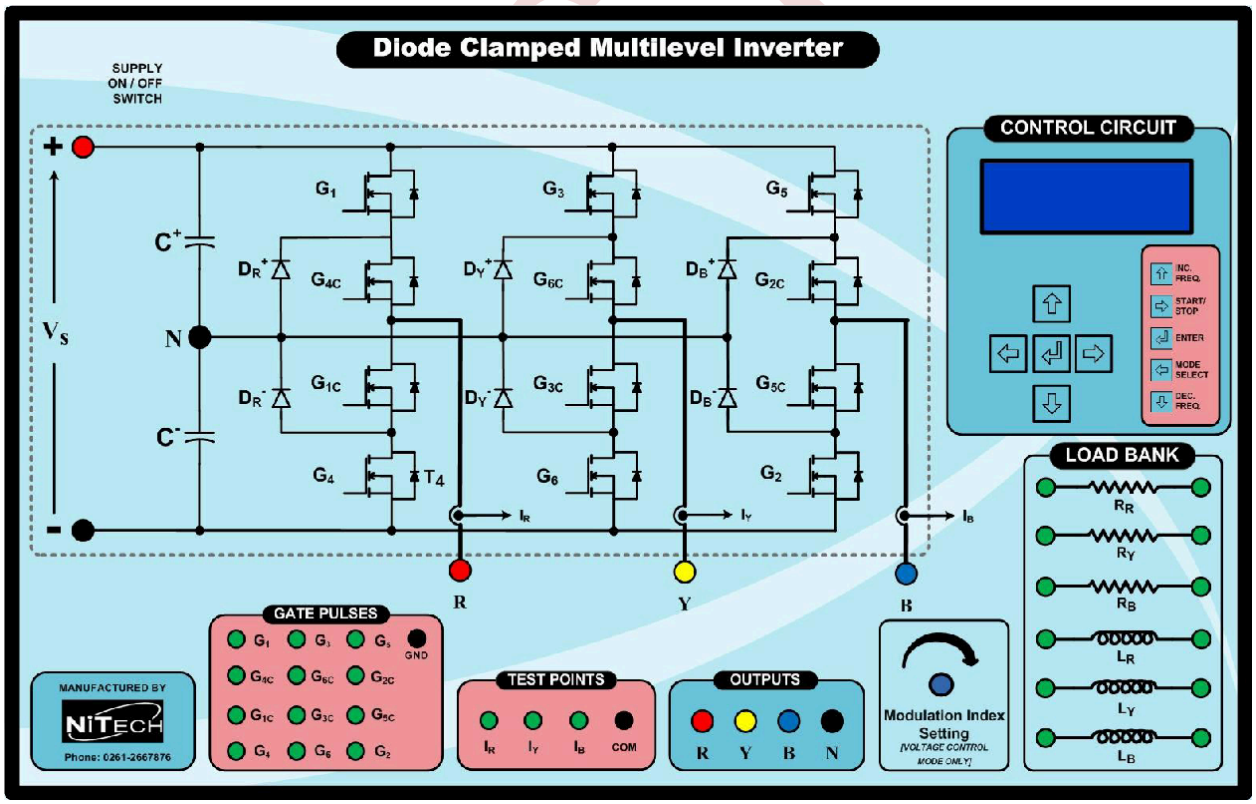
EXPERIMENT NO: **DATE:**

AIM: TO STUDY & PERFORM MULTILEVEL INVERTER IN SQUARE WAVE MODE WITH R-L LOAD

APPARATUS:

Multilevel inverter trainer kit, Oscilloscope, Connecting probes, Multi-meter.

CIRCUIT DIAGRAM:



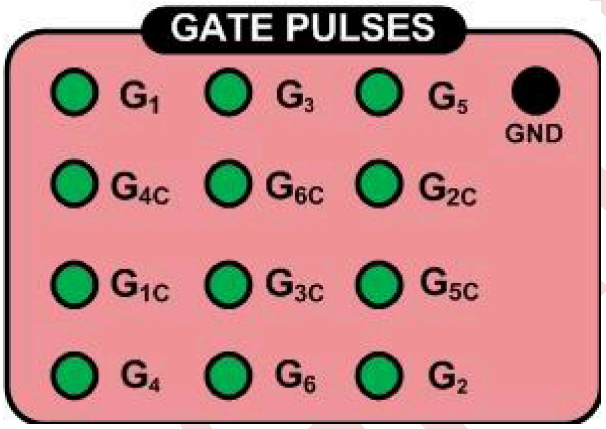
(Practical View)

FRONT PANEL DESCRIPTION

Control supply:

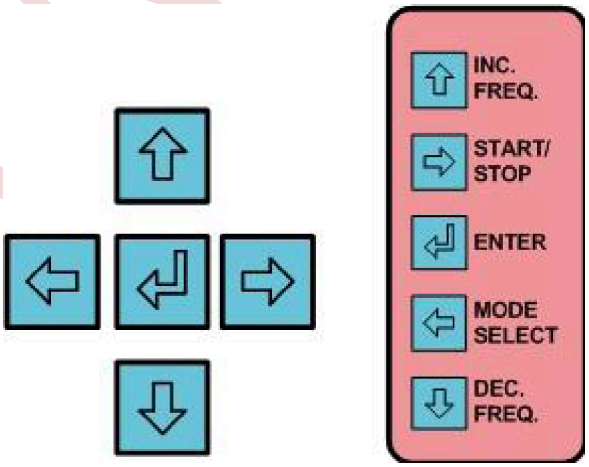
It is a power on/off switch for the supply to the control and power circuitry. Via plugging 230V, 50Hz AC source to the kit and closing this switch, user can provide supply to the unit.

Control circuit:



Gate pulses of 12 devices are available in this section. Following is the description of different waveform test points. GND is the reference point for observing gate pulse waveforms.

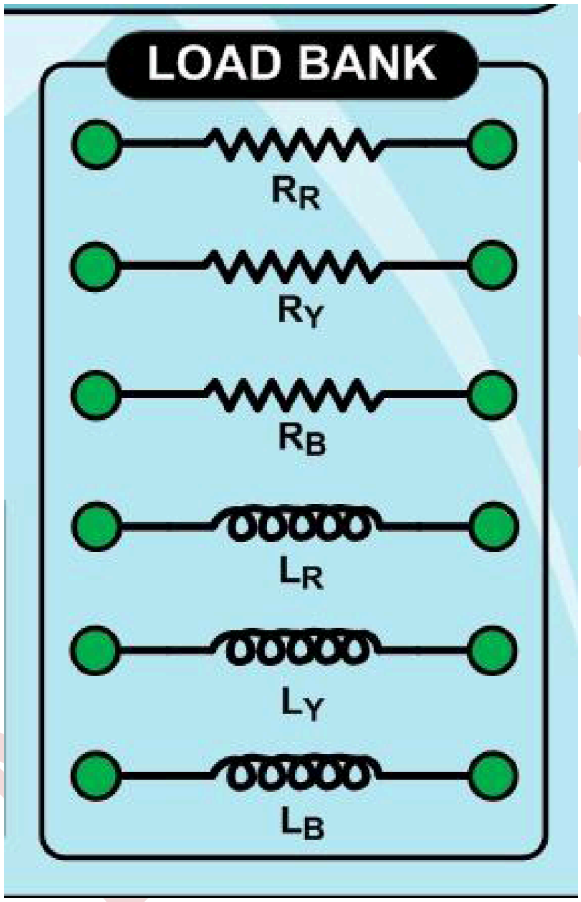
Control switch:



MODE SELECT arrow key is used to change the operating mode i.e. Square wave, V Control (SPWM) (sinusoidal pulse width modulation), V/F Control (SPWM), V Control (SVM) (Space Vector Modulation), V/F Control (SVM) mode. The START/STOP key is used to start the

different mode. These control signals provides optical isolation and is processed through gate driving circuit before actually connected to the power device. INC.FREQ. and DEC. FREQ. keys
are used to increase and decrease frequency of output voltage signal for all mode of operation. ENTER key is use to set the frequency.

Load bank:



Load bank provides three phase resistive bank and three inductors. The resistive load RR, RY, and RB each are having value of 50Ω, 25W. Also the inductive loads LR, LY, LB each having value 120mH. Each load is available with individual terminals.
By interconnection one can form balanced three phase R-load and R-L load either in star or in delta configuration.

THEORY:

Selective Harmonic Elimination (Square Wave)

SPWM technique is one of the most popular modulation techniques among the others applied in The Fourier series expansion of waveform with different notches is given by

$$v_{an}(\omega t) = \sum_{k=1,3,5,\ldots}^{\infty} \frac{4V_{dc}}{k\pi}(\cos(k\alpha_1) + \cos(k\alpha_2) + \cdots + \cos(k\alpha_s))\sin(k\omega t)$$

The expression for the fundamental voltage in terms of switching angles is given by

$$\frac{4V_{dc}}{\pi}(\cos(\alpha_1) + \cos(\alpha_2) + \cdots + \cos(\alpha_s)) = V_1$$

For controlling fundamental voltage and 'n' numbers of harmonics, 'n+1' notches are required. One degree of freedom is used to control the magnitude of the fundamental voltage and the remaining 'n' degrees of freedom are used to eliminate 'n' numbers of harmonics.

PROTECTION:

1. 3A fuse is provided to control the load current.

2. Internal load bank avoids overloading because of external load connection.

3. Power circuit is fed with isolated DC supply which helps for isolated voltage and current waveform viewing on oscilloscope.

4. Proper isolation is provided between the gate firing circuit and power circuit.

5. Proper heat dissipation arrangement is provided for power device to avoid excessive heating.

PRECAUTIONS:

1. All the connections are to be made with the main supply switch is in OFF condition.

2. Do not short load terminals.

3. Before switching ON the supply ensures that proper rating fuse is connected.

PROCEDURE:

1. Follow the general practical procedure.

2. Connect 'R-L load' from LOAD BANK into Y-connection.

3. Connect oscilloscope and multi-meter as AC (RMS) Voltmeter across load terminal.

4. Start trainer kit and select "Square wave" mode from menu on the LCD. Press START to start inverter.

5. Make supply switch ON and observe the load voltage output waveform on oscilloscope. Also measure its RMS value and frequency. Vary frequency and take readings.

OBSERVATION TABLE:

Supply Voltage (DC) Vs = _____ V.

Sr. No.	Frequency (Hz)	Phase Voltages (V)			Line Voltages (V)		
		V_{RN}	V_{YN}	V_{BN}	V_{RY}	V_{YB}	V_{BR}

CONCLUSION:

SIGN: **MARKS:**

VOLTAGE CONTROL IN MULTILEVEL INVERTER

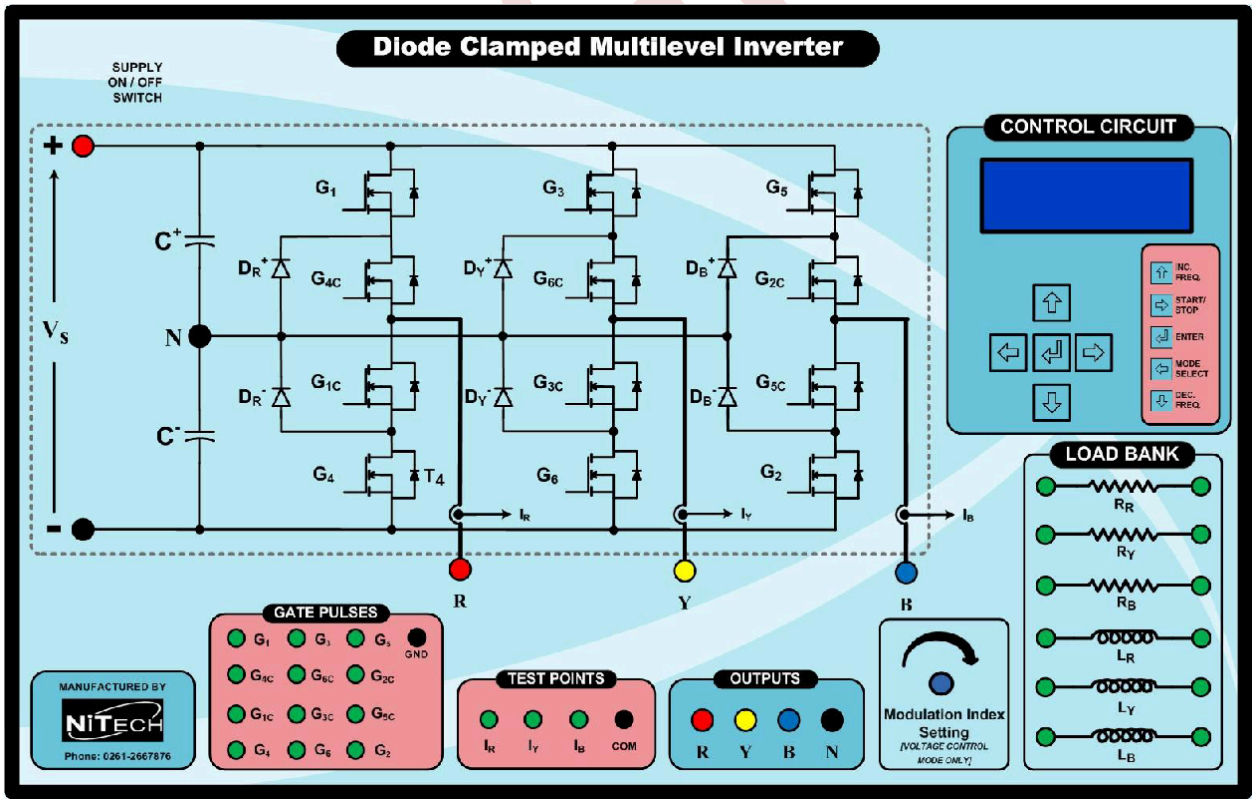
EXPERIMENT NO: **DATE:**

AIM: TO STUDY & PERFORM VOLTAGE CONTROL IN MULTILEVEL INVERTER CONTROLLED WITH SPWM & WORKING WITH R-L LOAD.

APPARATUS:

Multilevel inverter trainer kit, Connecting probes, Oscilloscope, Multi-meter.

CIRCUIT DIAGRAM:



(Practical View)

THEORY:

SPWM technique is one of the most popular modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to generate gate signals for the switches of inverter. Power dissipation is one of the most important issues in high power applications. The multi-carrier SPWM control methods also have been implemented to increase the performance of multilevel inverters and have been classified according to vertical or horizontal arrangements of carrier signal. The sinusoidal SPWM is the most widely used PWM control method due to many advantages including easy implementation, lower harmonic outputs according to other techniques, and low switching losses.
In SPWM control, a high frequency triangular carrier signal is compared with a low frequency sinusoidal modulating signal in an analog or logic comparator devices. The frequency of modulating sinusoidal signal defines the desired line voltage frequency at the inverter output. In SPWM control technique, the output voltage is obtained in linear modulation range,

$$V_{AB} = V_{BC} = V_{CA} = m_i \frac{\sqrt{3}V_d}{2} \quad 0 < m_i \leqslant 1$$

PROTECTION:

1. 3A fuse is provided to control the load current.

2. Internal load bank avoids overloading because of external load connection.

3. Power circuit is fed with isolated DC supply which helps for isolated voltage and current waveform viewing on oscilloscope.

4. Proper isolation is provided between the gate firing circuit and power circuit.

5. Proper heat dissipation arrangement is provided for power device to avoid excessive heating.

PRECAUTIONS:

1. All the connections are to be made with the main supply switch is in OFF condition.

2. Do not short load terminals.

3. Before switching ON the supply ensures that proper rating fuse is connected.

PROCEDURE:

1. Follow the general practical procedure.

2. Connect 'R-L load' from LOAD BANK into Y-connection Connect oscilloscope and multi-meter as AC (RMS) Voltmeter across load terminal.

3. Start trainer kit and select "V Control SPWM" mode from menu on the LCD. Press START to start inverter.

4. Make supply switch ON. For three different values of frequency change the modulation index, Observe the load voltage output waveform on oscilloscope. Also measure its RMS value and frequency. Vary frequency, MI and take readings.

OBSERVATION TABLE:

Supply Voltage (DC) Vs = _____ V.

Sr. No.	Frequency (Hz)	M.I.	V_{RN}	V_{YN}	V_{BN}	V_{RY}	V_{YB}	V_{BR}
1								
2								
3								

CONCLUSION:

_____

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SIGN: **MARKS:**

CLASS E RESONANT INVERTER

EXPERIMENT NO: **DATE:**

AIM : SIMULATION OF CLASS E RESONANT INVERTER & ITS PERFORMANCE

THEORY : In class E converter, the load is supplied through the supply tuned series-resonant circuit shown in fig. this result in essentially sinusoidal current i_0,the input to the converter is through a sufficiently large inductor to allow the assumption that in steady state.

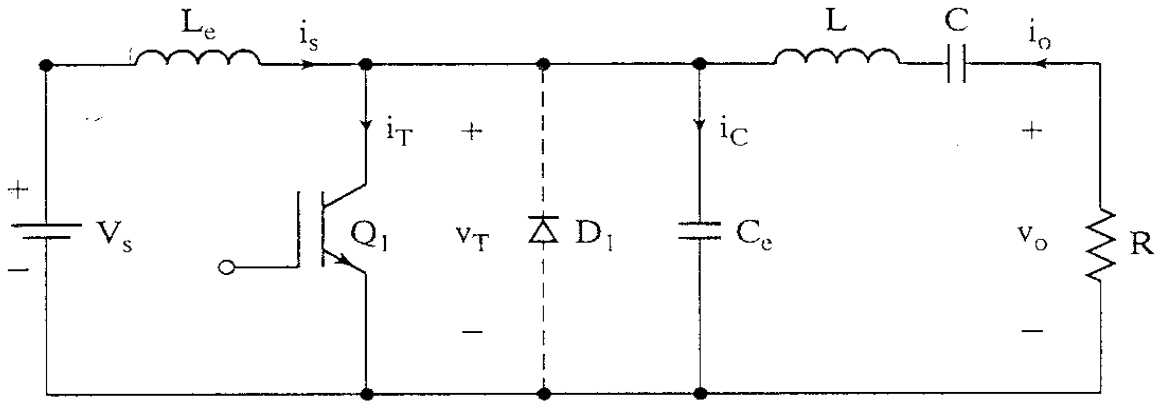

Fig 1 Class E Resonant Converter

The input to the converter is a dc current source i_s as shown in figure. Where current magnitude depend on the power output. The wave forms are as shown in figure. For an optimum mode ,when the switch is on, l_D+l_0 flow through the switch, as shown in fig. when the switch is turn off, because of capacitor C_1,the voltage across the switch build up slowly,

thus allowing a zero voltage turn off the switch. with the switch off. the oscillating circuit as shown in fig. where the voltage across capacitor C_1 build up, reach its pick ,and eventually comes back to zero ,at which instant the switch is turn back on. A class E converter operate at a switching fs, which is slight higher than the resonant frequency $f_0 = 1/(2\pi\sqrt{LrCr})$ $\pi\sqrt{LrCr})$ during the interval when the switch is off the input supplies power to the circuit since V_t is positive. Another observation that the average value of $V_t = V_d$, if i_0 is assumed to be purely sinusoidal the average voltage across the load resistance R is 0.the average voltage across L_r is also 0 in steady state therefore C_r block the dc voltage V_d in addition to providing the resonance circuit

The advantage of classic converter is the elimination of switching losses and the reduction in EMI; also it is a single switch technology and produces a sinusoidal output current. Significant disadvantage are high pick voltage and current associated with the

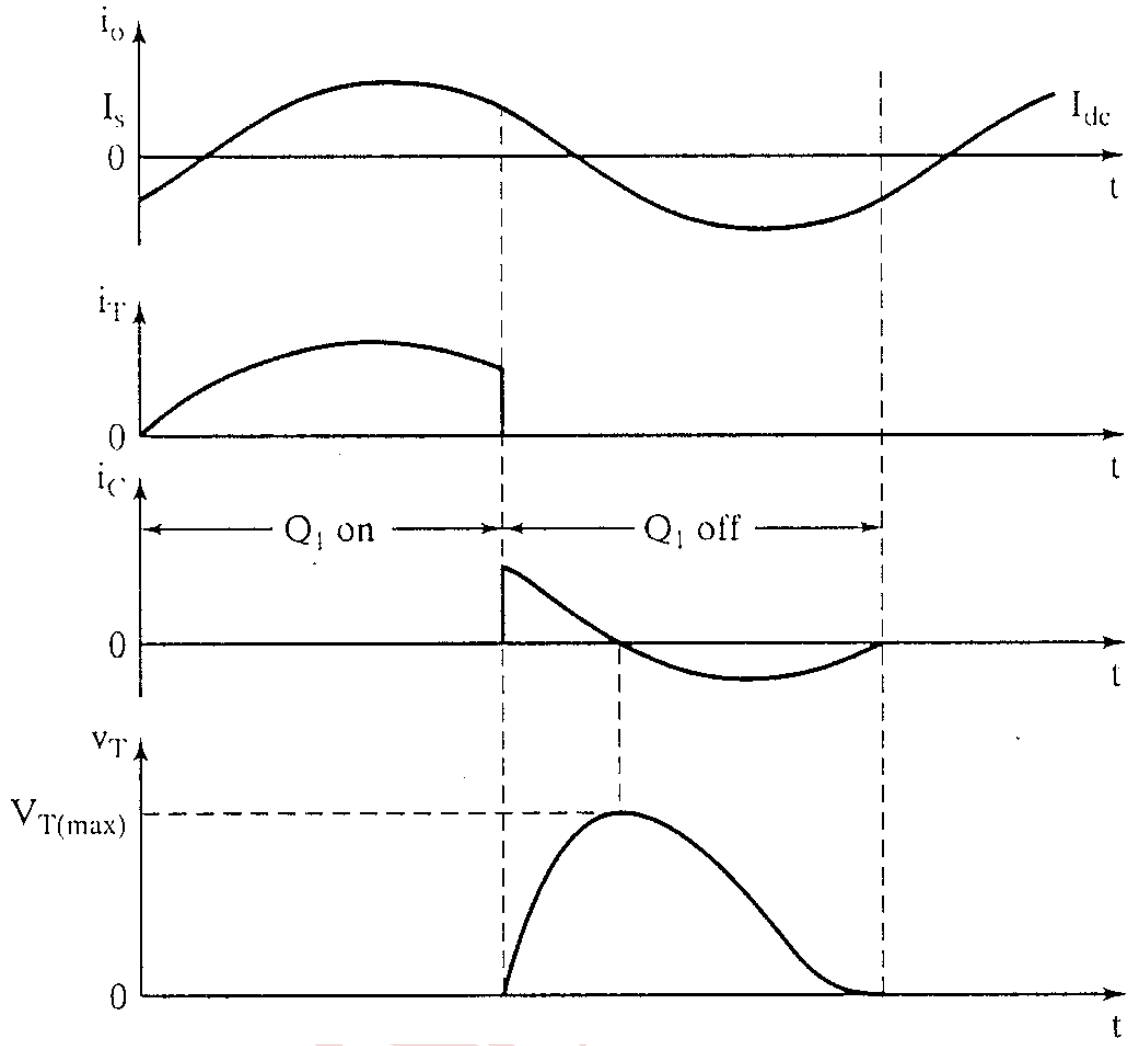

Fig 2 waveform for class-E Resonant Inverter

switch and the large voltage and currents through the resonant L_c elements. it is possible to obtain a dc-dc voltage conversion by rectifying the output current.

$L_e=0.4001R/\omega_s$

$C_e=2.165/(R\ \omega_s)$

$\omega_s L - 1/(\omega_s C)=0.3533R$

Simulink Model of Class E Resonant Inverter

Fig 3 shows the simulink model for a Class E resonant Inverter.Fig 4(a) are sketched waveform for capacitor current I_c, Fig 4(b) is I_0 & I_d, Fig 4 (c) are switct current I_T & switch voltage V_T.

Specification:

i/p voltage V_d=12V. **L_{dc}=350e-5**

C_{dc}=1.38e-6 **C_R=0.0958e-6**

L_R=445.63e-6 **f=25000Hz**

$R_{load}=3\Omega$

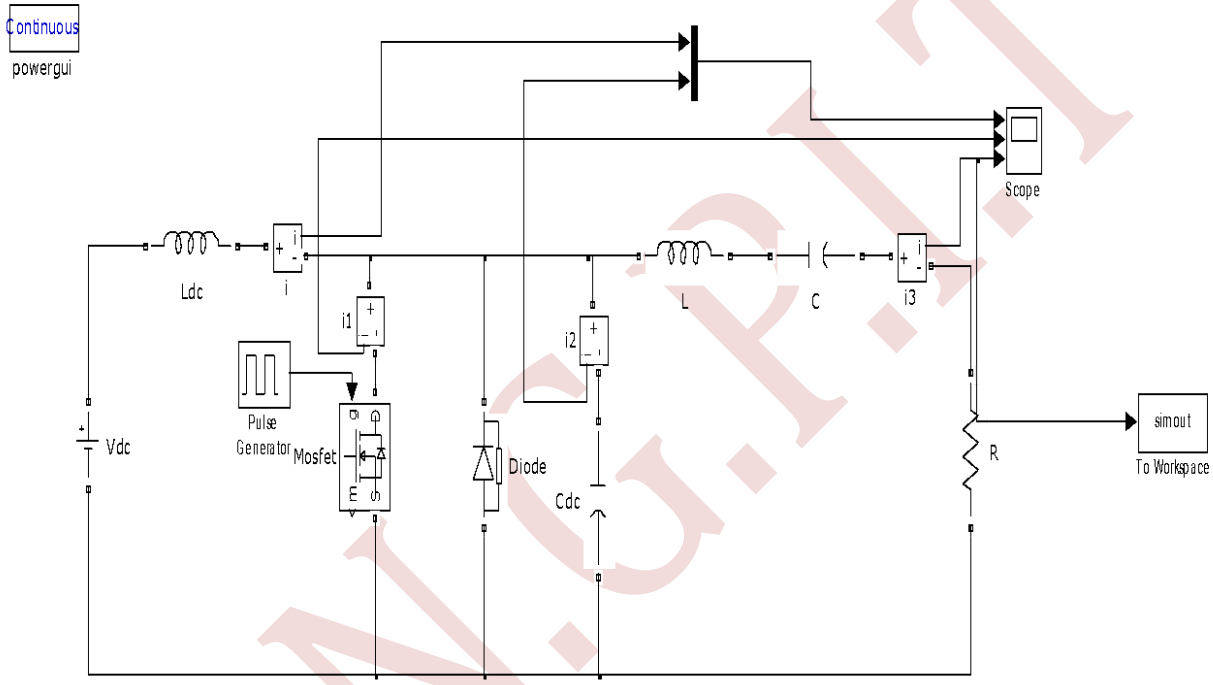

Fig 3 simulink model of class E resonant Inverter

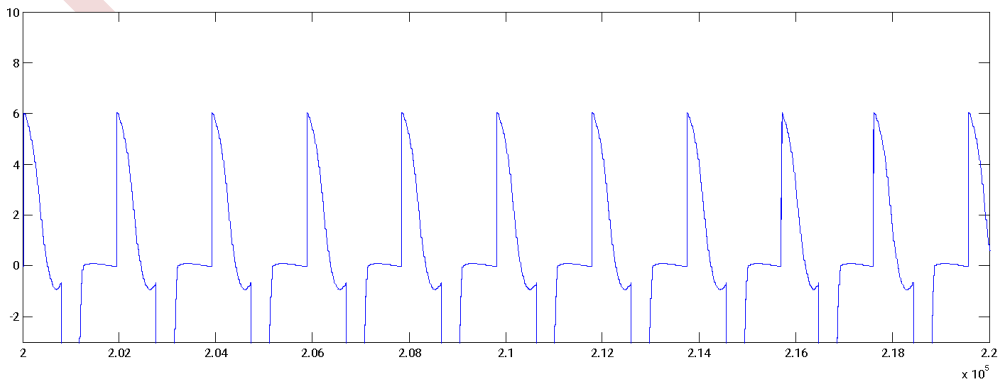

Fig 4 (a) Capacitor current I_c

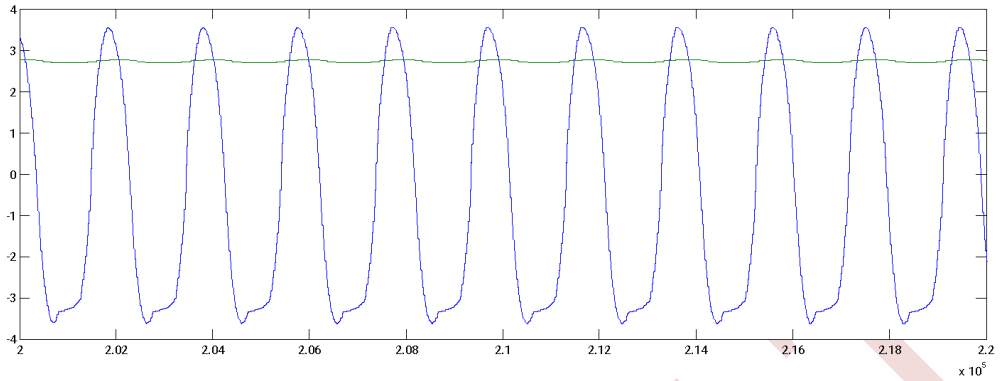

Fig4 (b) load current I_0 & I_d

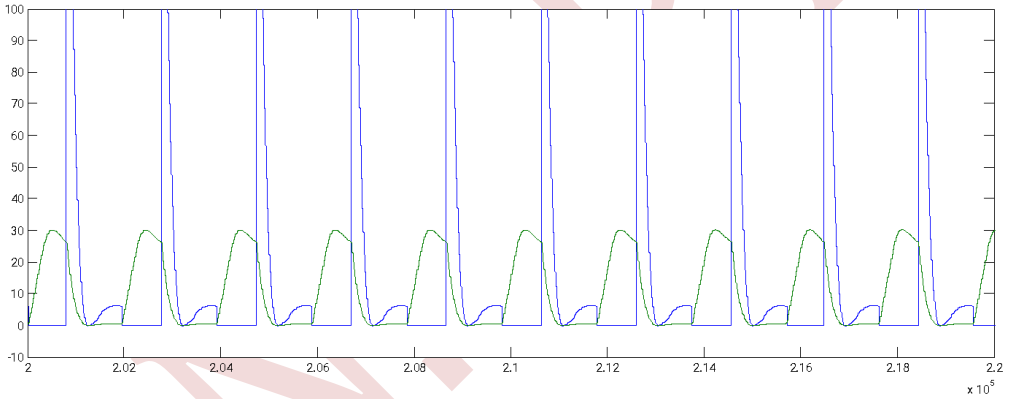

Fig 4(c) Switch current I_T & V_T

Result:

CONCLUSION:

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SIGN: **MARKS:**

L-TYPE ZCS CONVERTER

EXPERIMENT NO: **DATE:**

AIM: SIMULATION OF L-TYPE ZCS RESONANT CONVERTER & ITS PERFORMANCE

THEORY:

The converter circuits which employ zero current switching is called ZCS Resonant converter. An L-type ZCS resonant converter is shown in figure(a).

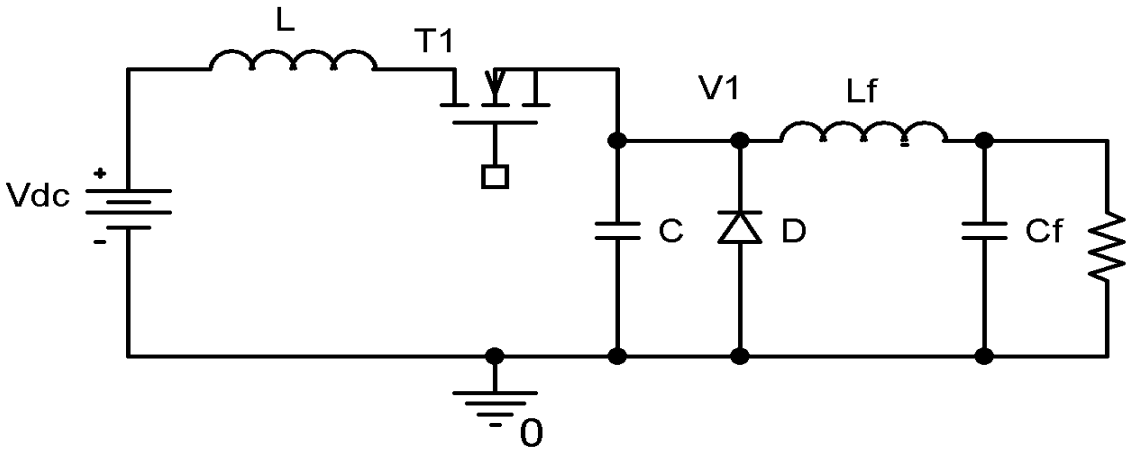


Fig 1 L-Type ZCS Resonant Converter

Initially inductor L_f is large so that load current Io is all most constant. Initially switch is open, current I_L=0 and voltage across capacitor Vc=0 and load current Io free-wheel through diode D.

MODE-1 (0≤t≤t1)

At t=0, When switch is on, as Io is flowing through diode, it appears as a short circuit across the diode Vd=0 and Vc=0. Hence, the supply voltage appears across L,so that it rise linearly and given by,

$I_L=(V_S/L)T$ $I_D=Io-I_L$

At $t=t_1$,$Io=I_L$

S0,$I_D=0$. So, diode turn-off and voltage across capacitor is Vc=0 is removed Ic=0

MODE-2 (0≤t≤t2)

In this mode, switch is on, diode is off. Beyond t1, I_L>Io, so their difference I_L-Ic flows through capacitor Cr, So its start change upto Vs. The inductor current is sinusoidal in nature. Vs is cosine in nature.

At t_1 , current I_L reaches to peak value

so Vc=Vs

At t_2 , I_L drops from its peak value to Io and capacitor voltage reaches to 2Vs.

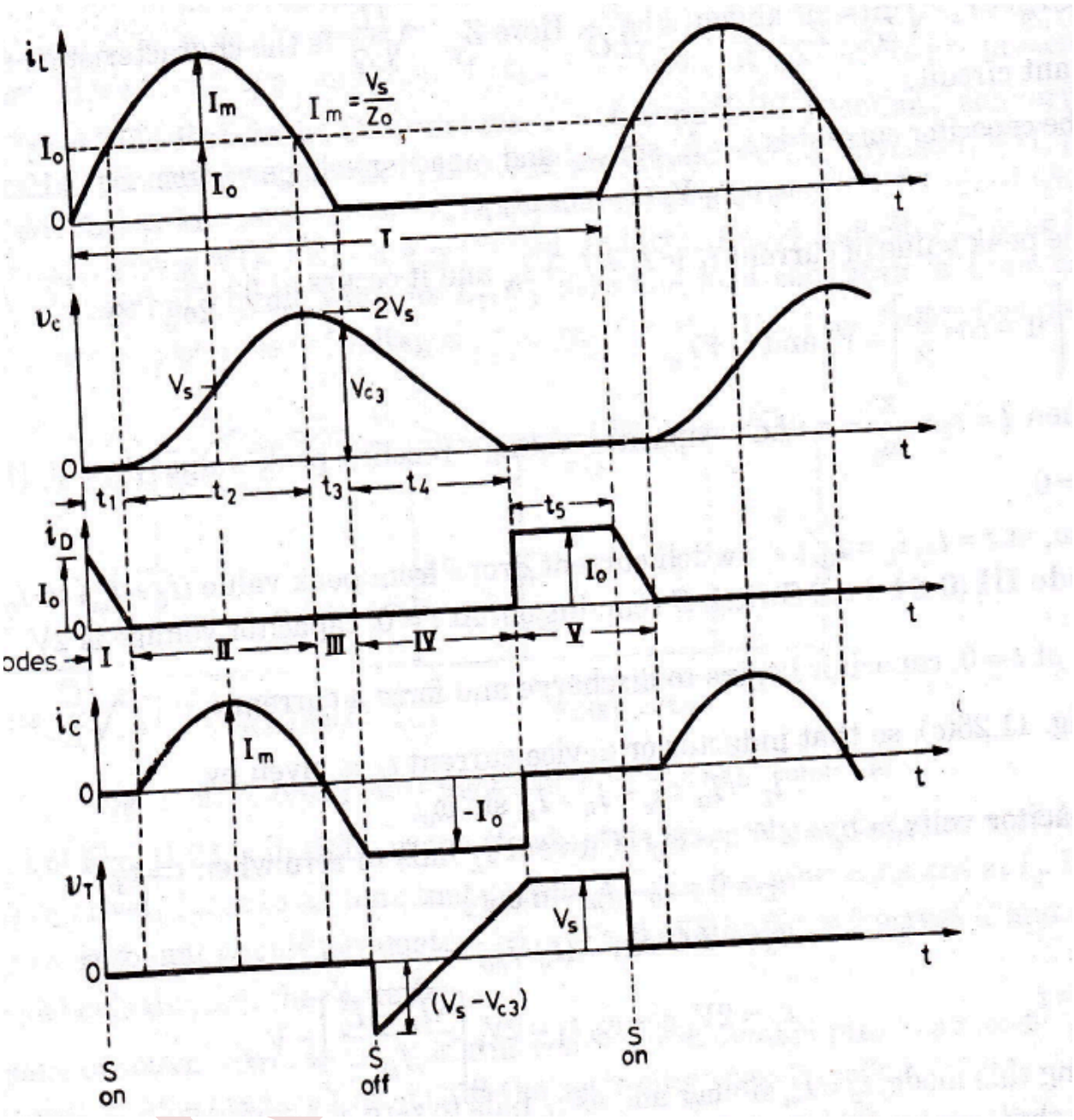


Fig 2 Waveforms for L-Type ZCS Resonant Converter

The inductor current I_L is given by

I_L=Io+Ic

I_L =Io+Im sin(ω_0t)

The capacitor current Ic= Im sin(ω_0t)

At t=t_2,

I_L=Io,Vc=2Vs,Ic=0.

MODE-3 (0≤t≤t3)

In this mode, switch is on at t3 and IL falls from Io to zero at t3.So switch is turn off at t3.

The inductor current I_L=Io-Im sin(ω_0t) & The capacitor voltage Vc=2Vs cos(ω_0t)

At t=t_3,Vc=2Vs.

MODE-4 (0≤t≤t4)

In this mode switch is turned off, capacitor starts to discharge and begin to supply the load current Io and is given by,

Vc= Vc_3-(Io/C)t

At t=t_4,capacitor voltage Vc=0,Ic=Io.

MODE-5 (0≤t≤t5)

When the capacitor voltage tends to become negative, that time Dm conducts and the load current Io freewheels through diode Dm. At t=t5,when the switch is turned on again and the cycle is repeated.

From the waveforms, it is seen that at turn on at t=0 (0≤t≤t1) switch current I_L=0. Therefore the switching loss $V_T I_L$ =0. Similarly, at turn off at t=t_3, I_L=0 and therefore switching loss $V_T I_L$=0.It shows that switching loss during turn on & turn off processes is almost zero. The peak resonant current Im=Vs/Zo must be more than the load current Io, otherwise the switch current I_L will not fall to zero and switch S will not get turned off.The load voltage Vo can be regulated by varying the period t5. It is obvious that longer the period t5, lower is the load voltage.

Calculation:

Taking,V_s=12V , Io =0.1A, T=0.02ms.

Assume that the intervals t_1 & t_3 are very small & x=1.5 .The maximum frequency occurs when t_5=0. So that $t_1=t_3=t_5=0$, $t_2+t_4=T$. From mode 4, $t_4=2VsC/Im$ and $x=(Vs/Io)(C/L)^{1/2}$

From above equation

$\pi(LC)^{1/2} +2VsC/Io = T$

then $(\pi Vs/xIo)C +2VsC/Io = T$

Taking this value

- V_s=12V , i_0=0.1A, T=0.02ms.
- We get C=0.0407e-6F.
- now $L= (Vs/xIo)^2C$=260.52e-6H.

Simulink Model of L-Type ZCS Resonant Converter

Fig 3 shows the simulink model for a L-Type ZCS Resonant Converter. Fig 4(a) are sketched waveform for Inductor current I_L & switching pulse 4(b)Capacitor current I_c 4(c) Capacitor Voltage V_c

Specification:

Supply voltage V_s=12V. o/p voltage V_o=4V

P_L=400mW $x=I_m/I_0=1.5$

o/p current i_0=0.1A Duty Ratio 20%

C=4.07e-8 L=2.6e-4.

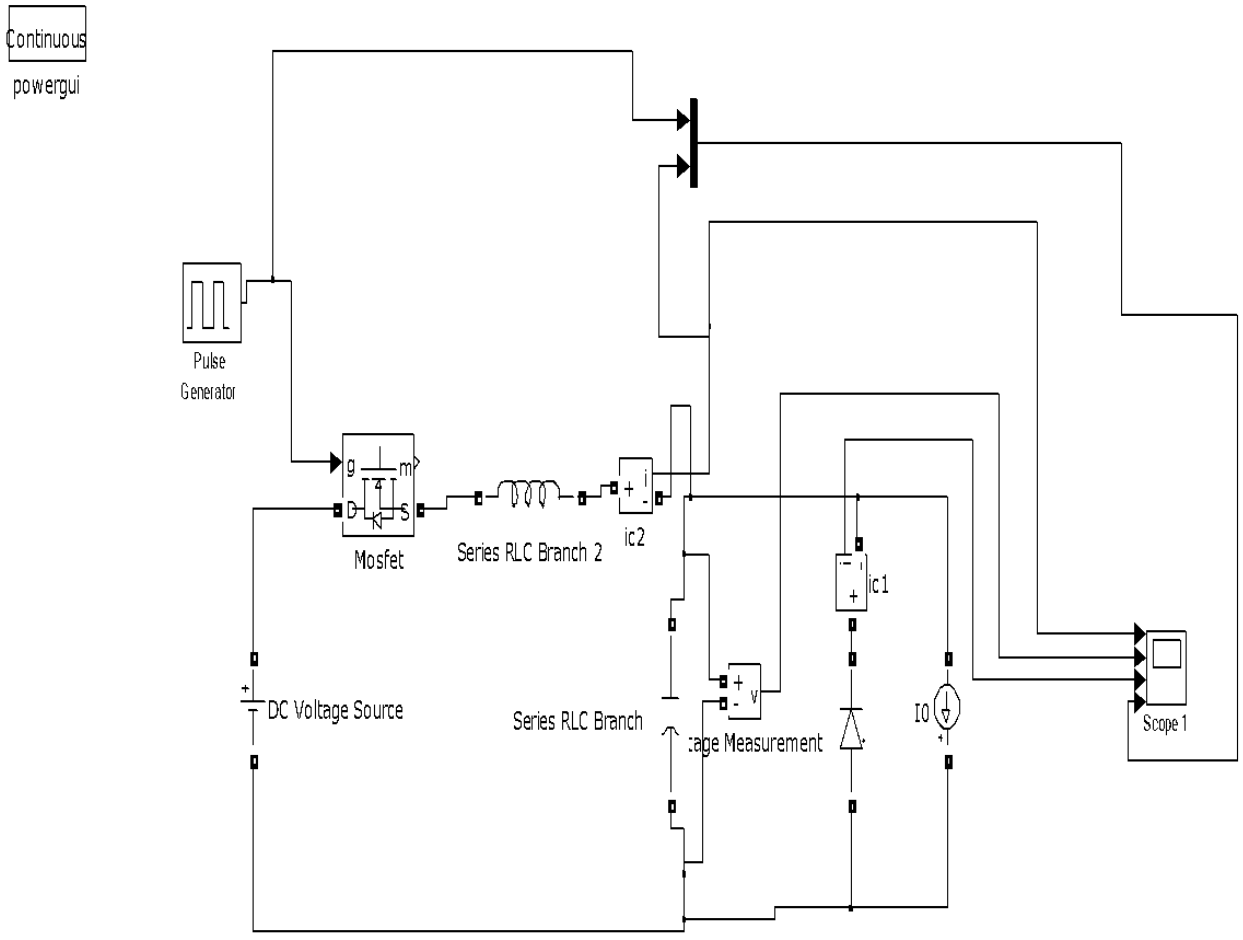
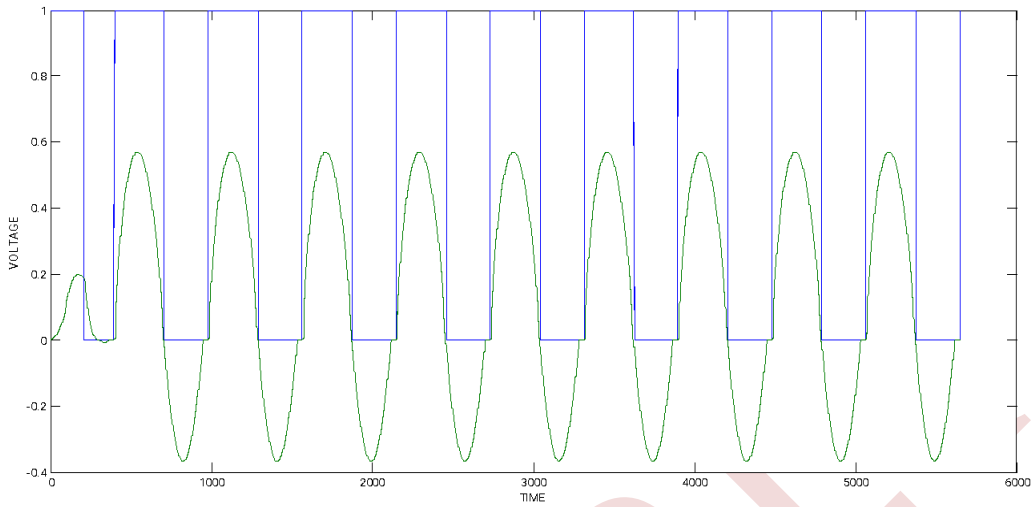
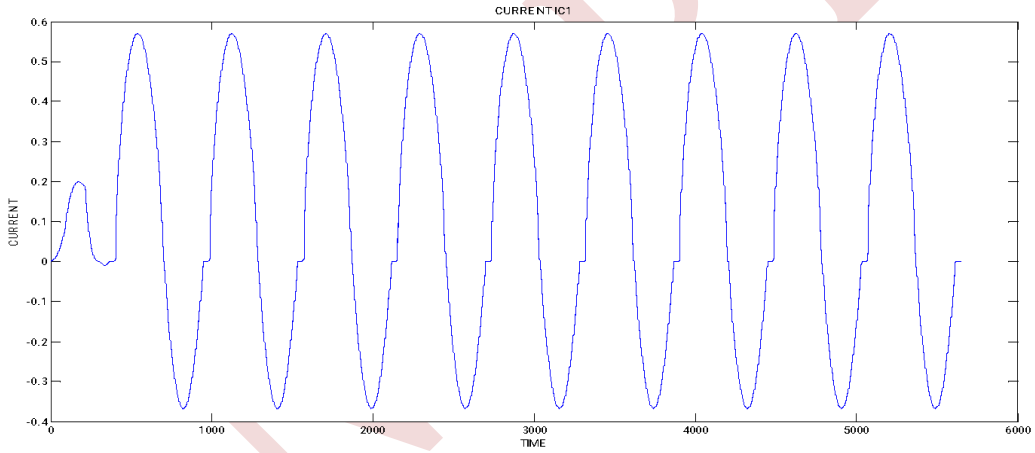
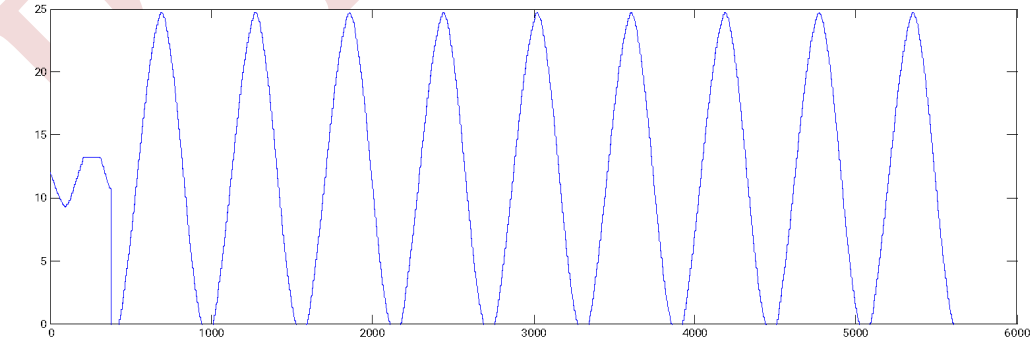


Fig 3 Simulink model of L-Type ZCS Resonant Converter







CONCLUSION:

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SIGN: **MARKS:**