

2025-12-10 Electrical Testing Session

<https://indico.physics.lbl.gov/event/3230/sessions/914/#20251210>

Action items

- Attach names and deadlines to action items <- botho by X-mas
- Set up SCIPP sensor test box at BNL
- Set up SCIPP UV treatment box at BNL+LBNL - which UV light to be used?
- Report US HBI-GUI problems to developers - Alex by 2026-02
- Speed up MTC temperature ramping at LBL - Botho Paschen 2026-01
- Evaluate grounding changes with 2nd LBL coldbox - Botho Paschen by 2026-03
- Send modules from BNL/LBNL to SCIPP for debugging
- Develop PS vs. AMAC current analysis (p-stop failure / resistor check)
 - Determine bleed resistance
- Investigate deionizing procedures more closely - Yoshi by 2026-01 (at least preliminary)
 - Correlate method/time vs. location of charge
 - > does it make sense to introduce a general air deionization step of bare sensors, what time is needed
- Merge coldjiblib stave efforts back
- Encourage ITSDAQ to have tagged version
- Have coordinated software versions used in US -> dedicated (rotating) testers of new versions?
- Dedicated testing slot at beginning of Friday meeting every other week

Sensor testing

- IV curve #1 descope at LBL, no failures in IV curve #2 since then
- SCIPP 8 sensor test being set up at LBL, seeing some increased noise but passing tests in most channels now
 - 8 sensors can be tested in ~40 min
- **BNL interested in commissioning a SCIPP sensor test box as well**

Hybrid testing

- Currently least stable part of electrical testing pipeline
- Hybrid burnin GUI has been adopted by all three US sites
- HBI-GUI better than previous system but still shortcomings
- Fuse-ID based ASIC assembly is a great feature
 - Has been observed to fail because of
 - Components not at the assembly DB institute

- Forgotten shipment
 - Missing chips in DB gelpack
 - Communication failure -> wrongly read fuse-ID
- Single failing ASIC assembly will prevent correct assembly for all following hybrids inside the crate
- Assembly failure is silent in GUI and can only be found from log
- **Various other problems to be collectively reported to HBI-GUI developer**
 - Checkmarks present for unused slots
 - Result checkmarks always red because power-cycle test not implemented in DB
 - FPGA needs frequent reflashing at BNL, occasional at SCIPP and LBL
- Frequent problems with hybrids necessitate manual interaction at beginning of burnin
 - Understanding which hybrids do not work properly is difficult
 - Checking connection test in ITSDAQ at LBL
 - Sometimes just a delay timing change is necessary, automatic procedure would be nice here
- Can be hazardous to fetch correct serial numbers for burnin each time
 - SCIPP proposal for enabling local names inside burnin GUI

Module testing

- Overall stably running
- Pre-TC test seen as necessary to weed out problematic modules
 - Routinely executed at BNL+SCIPP
 - Takes ~2 hours
 - IV curve + Full test (done via GUI by everyone?)
 - Proposal for faster test by LBL: fast ramp, -50 V steps, to -100 V (or -550 V?) and only response curve test
 - Would be nice to have automated
- Slow-down factors are temperature ramping and HV ramping
 - Temperature ramping agreed to be done at fastest possible speed (~5.5 C/min) instead of nominal 2.5 C/min
- LBL coldbox grounding and jig changes to be re-verified with 2nd coldbox
- How long does full TC takes (~19h with fast chiller ramp)?

Debugging

- Schedule does not foresee (allow for) debugging during production as long as yield is acceptable
- Now, debugging is good to do when there is time to understand possible problems, modules, setups, and train new personnel
- **SCIPP offers to take any debugging-worthy modules from BNL+LBL**

- Pinhole tests: not standard, instructions below
- P-stop shorts: show up as extra PS current not seen by AMAC
 - So far caught by HV PS compliance and channel shutdown or by eye
 - > **Should develop test/analysis script**
- Stuck charges (see below)

Pinhole test instructions:

- **Fast, can be done in seconds, but doesn't detect all pinholes**
- **Only for fun. Not recommending to fix pinholes as part of standard QC**
- https://gitlab.cern.ch/atlas-itk-strips-daq/itsdaq-sw/-/blob/master/macros/AMACStar_PinholeCheck.cpp?ref_type=heads
 - LV on, no need for HV. Configure modules as usual
 - source RUNITSDAQ.sh
 - .L macros/AMACStar_PinholeCheck
 - AMACStar_PinholeCheck(-1) (or replace -1 with AMAC number)
- The output messages come with a diagnosis that is more or less self-explanatory
- Results are saved in a json file
- There is also another version in merge request here which attempts to detect the chip it is on: https://gitlab.cern.ch/atlas-itk-strips-daq/itsdaq-sw/-/merge_requests/1647
 - Instructions are the same but just use AMACStar_PinholeLoc instead

Stuck charges

- Problem at all sites
- Exact moment of introduction not always clear
 - According to Vitaliy it is expected that charges cannot stick to surface longer than ~months
 - But LBL sees central charge deposits despite not using central pickup tools
 - BNL sees charges persist for 4 months in dessicator
- Important to properly deionize tools and test frames before assembly
- Probably important to deionize sensors before gluing
- **SCIPP UV treatment box to be set up at BNL + LBL**
 - Hunting for lab conforming UV lights
- UV method in most cases clears charges in 1-4 hours
 - Sometimes 30 hours needed
 - Spacer has to be taken off because it gets damaged
- Time to clear charges with fan method unclear
 - Usually ~1h applied by SCIPP
 - LBL reported success for 'away' region charges in ~10 minutes

-> Correlate these times with location of charge better to come up with general procedure

Software

- No proper versioning of ITSDAQ -> encourage them
- Have coordinated updates / versions in US
 - Dedicated person/setup to test new versions and decide about updates
- Which software to monitor?
 - ITSDAQ and coldjig most importantly
 - What about grafana + influx
 - FPGA firmware