BANGALORE INSTITUTE OF TECHNOLOGY
K R ROAD, V V PURA, BENGALURU-04

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

COURSE OBJECTIVES AND OUTCOMES-2017-21

Course Title: Advanced Computer Architectures	**Course Code: 17CS72**
No. of Lecture Hrs./Week : 04	**Exam Hours : 03**
Total No. of Lecture Hrs. : 50	**Exam Marks : 60**

Prerequisites

1. Computer Organization (17CS34).
2. Microprocessors and Microcontrollers(17CS44)

Course Learning Objectives

This course will help students to achieve the following objectives:

1. Understand the evolution of Computer Architecture (Hardware and Software).
2. Understand the types of processors and their scalability.
3. Measure the performance of the architecture in terms of right parameters.
4. Summarize parallel architecture and software used for them.

Course Outcomes

At the end of the course students should be able to:

1. Understands the concepts of parallel computing and hardware technologies.
2. Analyse linear and non-linear pipeline processors.
3. Compare and contrast the parallel architectures.
4. Illustrate parallel programming concepts.

CO-PO MAPPING-2017-21

	PO 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12		PSO1	PSO2
CO1	1	2	1	1											
CO2	1	2													
CO3	2	2	2												2
CO4			2	2											

CO-PO MAPPING JUSTIFICATION

17CS72	CO1	PO1	1	Apply the knowledge of fundamentals of computer science & engineering in designing processor, cache and memory.
		PO2	2	Apply the knowledge to analyze the problem and design the system.
		PO3	1	Apply and implement an algorithm for dynamic instruction scheduling to enhance the performance of the processor.
		PO4	1	Conduct investigation and research using algorithms to provide valid conclusions.
	CO2	PO1	1	Apply the knowledge of execution of an instruction within memory using different pipelining techniques.
		PO2	2	Analyse the performance of a system using linear and non-linear pipeline processors
	CO3	PO1	2	Apply knowledge on the design of pipelined processors and analyze their performance.
		PO2	2	Analyze the hurdles in the pipeline
		PO3	2	Design the pipelined processor of various stages.
	CO4	PO3	2	Implement the super scalar techniques.
		PO4	2	Design a system using a multi vector multiprocessor.

CO-PSO MAPPING JUSTIFICATION

17CS72	CO3	PSO2	2	Graduates are able to design and develop software for parallel programming.

Faculty In-charge Course Coordinator Module Coordinator IQAC Programme Coordinator